

Doctoral Dissertation

Hardware Implementation of Signal Processing in Smart Antenna Systems for High Speed Wireless Communication

(高速移動通信を実現するスマートアンテナ技術の実用化における
信号処理部の実装に関する研究)

Submitted on

December 15, 2004

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博士論文

高速移動通信を実現する
スマートアンテナ技術の実用化における
信号処理部の実装に関する研究

平成16年12月15日提出

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Abstract

Smart antennas basically attempt to enhance the desired signal power and suppress the interferers by beamforming toward the DOA (direction-of-arrival) of the desired signal and nullsteering in the case of the interferences' DOAs in line-of-sight (LOS) situation. This paper considers a smart antenna system for cellular base station application. The signals at the base station are received through the scattering process from the local scatterers around the mobile station because the antenna is usually deployed higher than surrounding scatterers. In this case, although the fading across the antenna elements spaced by $\lambda/2$ is highly correlated, the AS is typically only a few degrees. Hence, the angle domain approach exploiting the DOA information can be useful. Moreover, only the DOAs are *commonly* useful channel information in both uplink and downlink channels of Frequency Division Duplex (FDD) systems where each link uses different frequency. This is because the average angular power spectrums in both links are almost identical. Thus, in an uplink, we can estimate the channel parameters with the received data that have passed the channel and apply the estimated DOA information to downlink beamforming. In a downlink channel, smart antenna transmitters can focus the energy to the desired user using the DOA information, and thus reduce the interference for other users. This is the most significant feature of the angle domain approach with DOA estimation.

This paper mainly aims at the practical and general applications of signal processing implementation of a smart antenna system for wireless cellular basestation systems. While theoretical studies are useful for analyses and simulation purposes, their implementation in real hardware and their validation with actual measurement data will be a meaningful challenge. This paper studies general signal processing independent of specific communication systems and hardware platforms. This paper proposes the smart antenna system based on the DOA estimation of incident signals, which includes fast DOA estimation and beamforming processors. The prototype system integrating signal processors on field programmable gate arrays (FPGAs) was manufactured and the evaluation testbed was configured. The prototype system employs an 8-element antenna array for 5 GHz band and an RF transceiver for each branch. The functionality of the baseband smart antenna processor was verified through hardware simulations and laboratory experiments. The entire hardware system, including RF, antenna arrays, and air interface, at both the transmitter and receiver configurations were also tested in a radio anechoic chamber.

Smart antenna systems, especially those based on DOA estimations, usually require high computational performance for array signal processing. Apart from the hardware complexity

of multiple transceivers and an impractically high cost, the limited performance of the signal processing devices has been a big obstacle to its realization. With the general Von Neumann architected processors such as the general micro processing unit (MPU) or the digital signal processor (DSP) with a single or few Multiplier-ACcumulators (MACs), it may be difficult to process a large amount of data from multiple antenna elements in real-time. They also inefficiently consume large power because they are not optimized for the specific purpose. In this paper, FPGAs are basically used as digital signal processors. Due to to the recent progress of Very Large Scale Integration (VLSI) technology, FPGAs have evolved from flexible logic design platforms to signal processing engines. FPGAs are now expected to be essential components of a software radio, which includes smart antenna technology, due to their high order of flexibility by SRAM-based structure and real-time processing capabilities. They are inherently suitable for high-speed parallel MAC functions. However, it is incorrect to assume that all DSP functions can always be implemented in FPGAs. Floating point operation is difficult to implement in FPGAs because a large amount of gate resources are wasted and the performance cannot be optimized. Further, processing involving matrix inversion (or scalar division) is also more suitable to a DSP or MPU platform. Therefore, FPGAs and DSP have coexisted for a long time, and a flexible platform usually includes their combination.

This paper presents the fixed-point processors of a fast DOA estimator and beamformer implemented with FPGAs. A DOA estimator incorporates unitary MUSIC algorithm, termed “Unitary MUSIC Processor (UMP).” Unitary MUSIC algorithm has a super resolution capability and is suitable for integration on logic circuit devices such as FPGAs. The techniques suitable for FPGAs, such as the eigenvalue decomposition by a cyclic Jacobi processor based on COordinate Rotation DIgital Computer (CORDIC) and spectrum computation by the spatial Discrete Fourier Transformation (DFT), can be exploited to optimize the fixed point arithmetic. This paper also proposes a novel beamforming technique with extremely low complexity that can use the estimated DOA information in the UMP. This beamformer computes the optimum weight vector with a simple convolution operation of precomputed beam and notch patterns; thus, it is able to provide a fast beamforming performance without any matrix inversion in conventional techniques.

The remainder of this dissertation is organized as follows. Chapter 2 introduces the developed hardware platforms of the smart antenna transceiver system and includes its implementation details. The hardware requirements in smart antenna technologies are also discussed. The benefits of FPGAs as array signal processors will be described in comparison with general-purpose DSP processors. The prototype transceivers were designed taking into consideration of the reconfigurable IF processing based on software-defined radio concept as well as the adaptive control of antenna beampattern. In order to implement this, the prototype transceivers are architected by low-IF super heterodyne with undersampling at receivers/harmonic band generation scheme in transmitters. In this chapter, the sampling jitter effect, which determines the maximum IF input frequency, is quantified based on measurements. The implementation of the smart antenna signal processing is described in Chapters 3 and 4. Chapter 3 presents the fast DOA estimation processor using unitary MUSIC algorithm. First, the design of a

fast eigenvalue decomposition processor based on a cyclic Jacobi method with the CORDIC technique is described. Second, the implementation of a fast DOA estimation processor termed UMP by FPGAs on a developed transceiver platform is described. The performance will be also quantified by fixed-point hardware level simulation. Chapter 4 proposes a novel beamforming technique with extremely low complexity and presents its performance and hardware implementation. Chapter 5 describes the experimental evaluation of the integrated system performance. The effects caused by real hardware imperfections, such as mutual coupling among antenna branches, are discussed and array calibration issues will be dealt with in this chapter. Finally, Chapter 6 summarizes the dissertation describing the contributions and remaining problems and outlines the future works to be examined.

Acknowledgments

I am deeply grateful to many peoples who supported me in their helpful comments and enlightening suggestions.

- First of all, my supervisor, Prof. Hiroyuki Arai always gave me the courage to carry out my research in Japan (aboard for me) as well as the technical and mental supports. I wish to express my gratitude to the committee members of Prof. Yasuo Kokubun, Prof. Ryuji Kohno, Associate Prof. Toshihiko Baba and Associate Prof. Koichi Ichige for helpful comments and careful reviews of this dissertation. I would like to express special appreciation to Associate Prof. Koichi Ichige for a plenty of advices and criticism about my research work. I also thanks to Associate Prof. Nobuhiko Kuga for his kind advise for my special research work.
- I would like to express deep thanks to Dr. Masahiro Fukuta, Mr. Hirotake Horiuchi and Dr. Li Chao Tan of Brains Corporation for financial support. I am also deeply grateful to Prof. Kwang-cheol Ko of Hanyang University, Seoul, Korea that Prof. Ko and Dr. Fukuta actually gave me the opportunity to study in Japan and participate in this research work. Dr. Fukuta also helped me the hardware support in designing and manufacturing testbed system and guided the hardware implementation skills.
- I would like to thank to Dr. Masahiro Karikomi of Nihon Dengyo Kousaku, Dr. Yoshio Ebine and Dr. Keizo Cho of NTT DoCoMo, Inc. and Dr. Koichi Tsunekawa of NTT Corporation for their research co-operation and helpful comments.
- My appreciation goes to my colleagues; Shintaro Muramatsu, Naoya Matsumoto, Tatsuo Fuji, Aiko Kiyono and Atsushi Nakajima for their reseach cooperation. I would like to thank to other colleagues in my research group; Yuki Inoue and Dr. Kohei Mori of Sony Corporation and Dr. Naobumi Michishita of National Defense Academy for their helpful discussion. I also would like to extend my gratitude to everyone in Prof. Arai, Prof. Ichige and new born Prof. Kuga laboratories. I would like to express my appreciation to Mr. Takehiro Miyamoto of Nihon Dengyo Kousaku for his helpful research co-operation.
- Finally, I owe special thanks to Shil my wife and Jaeweon my lovely son for their patience and understanding. And I also would like to thank my family including my parents in Korea for continuous encouragement.

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Chapter 1

Introduction

1.1 Background

In recent years, wireless communication systems have progressed greatly and the market, especially for the cellular phone, has witnessed explosive growth. Moreover, as the demand for multimedia services increases, a wider bandwidth of information will be required for next-generation wireless systems. These systems will be allocated at a higher frequency band because a number of useful frequency bands have already been allotted to and are occupied by existing systems. In order to accommodate a larger number of subscribers and to provide better quality services, it is necessary to increase the channel capacity. Further, the technologies required for power saving and efficient frequency reusability will be necessary for various multimedia services.

In fact, multipath fading, which is typically caused by a reflection from any physical structure, is an unavoidable phenomenon in wireless communication environments, because the signals are usually propagated through a multipath, as shown in Fig.1.1 [3]. When passing through a multipath, the signals are delayed and out of phase from the signals passing through a direct path; this causes the signal strength to be weakened at the receiver, thus reducing the receiving quality. A wider band and higher transmission rate will make this a more critical problem in the improvement of the quality of service in next-generation communication. Many solutions have been proposed to resolve this problem. In fact, the flexible configuration of the receiver and transmitter is important as a response to the signal environment that recognizes spatial channel profiles as well as temporal ones. As an example, spatial diversity techniques using composite information from the array to achieve average signal-to-noise ratio of spatially separated antenna, thus minimizing undesirable fading effects of multipath propagation, have been studied in many applications.

There exists another problem that is caused by multipath propagation. Delay spread is the difference in propagation delays among the multiple paths. It leads to inter-symbol-interference (ISI) that limits the maximum data rates. Frequency-selective fading occurs if the delay spread is equal to or larger than the inverse of the signal bandwidth.

The third major limitation in wireless communication system is referred to as co-channel interferences (CCIs). In the case of the time division multiple access (TDMA) system, such as

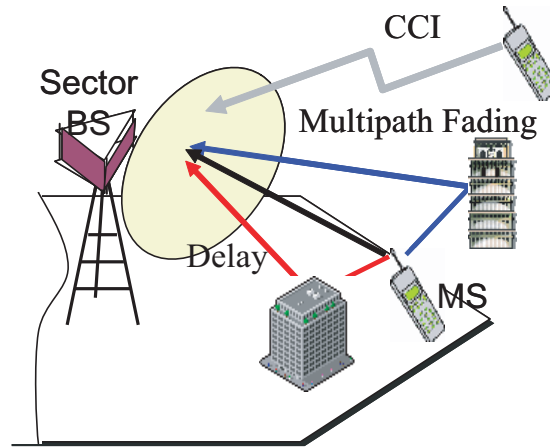


Fig. 1.1: Wireless cellular propagation environment.

the Japanese personal digital cellular (PDC) systems, IS-136, and European Global System for Mobile communications (GSM), the CCIs are primarily caused by frequency reuse; this implies that the spectrum allocated for the system is reused multiple times in neighboring cells. The problem is that the signals received by a base station and a mobile handset usually contain a signal component that has originated from more distant cells as well as a signal component of the desired channel data from the current cell. CCIs degrade the carrier-to-interference power ratio (CIR); thus, the system capacity will be limited by more frequent handoffs and reduced connectivity.

In order to cope with these inherent problems in wireless communication systems, smart antennas having multiple antennas have been proposed as a very promising technology to mitigate multipath fading and reject CCIs by efficiently exploiting the spatial domain signal processing; spatial domain signal processing is the next frontier of the resources of wireless systems for frequency, time, and code domain. Smart antennas can extend the capabilities of the next-generation systems to provide customers with increased data transmission throughput for high-speed multimedia applications.

1.2 Wireless Communication Systems

Wireless communication technologies have progressed greatly from the 1980s, as shown in Fig.1.2. This section presents a brief history of the wireless communication systems and provides an outlook into the future systems.

In the first generation (1G) systems, analog systems such as advanced mobile phone system (AMPS) and total access communications system (TACS) grew rapidly in the 1980s and are still available today. These systems use frequency division multiplexing to divide the bandwidth into specific frequencies that are assigned to individual calls.

The second generation (2G) systems introduced in the mid-90s are still used today. The second generation (2G) systems are digital and use either TDMA or code division multiple access (CDMA) methods. The Japanese PDC and European GSM are 2G digital systems with

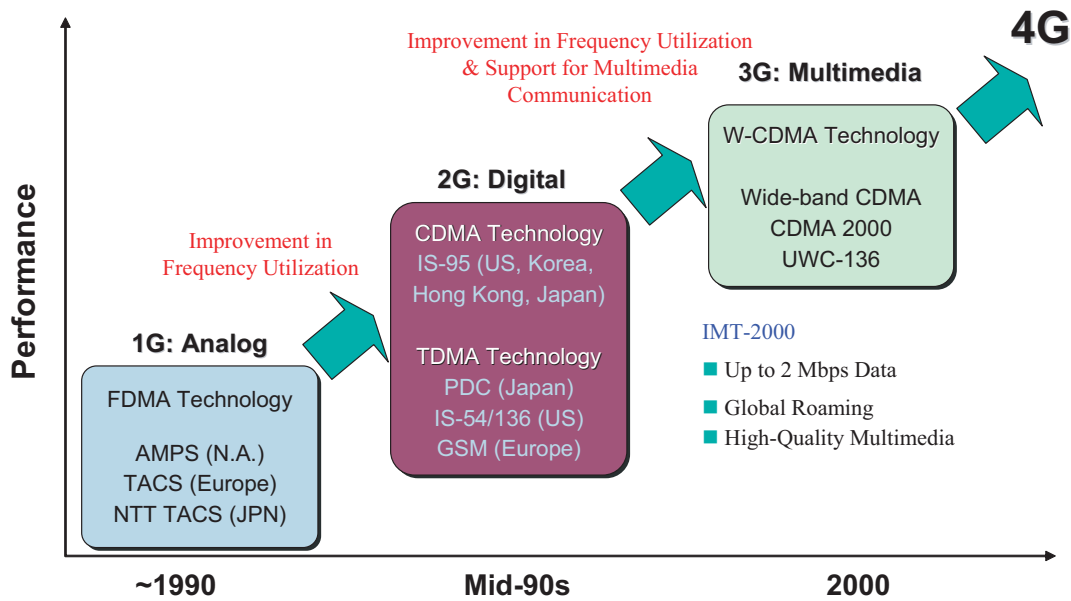


Fig. 1.2: Wireless cellular communication system roadmap.

their own TDMA access methods. On the other hand, the cellular systems in U.S.A., Korea, and Japan, use CDMA technology. The 2G digital services began appearing in the 1990s, providing expanded capacity and various unique services.

“Third generation (3G)” has become an umbrella term to describe cellular data communications with a target data rate of 2 Mbits/sec (actually 64 ~ 384 Kbps). The International Telecommunication Union (ITU) originally attempted to define 3G in its IMT-2000 (International Mobile Communications-2000) specifications that specified global wireless frequency ranges, data rates, etc. However, a global standard was difficult to implement due to differing frequency allocations around the world and conflicting inputs. Therefore, three operating modes were specified by WCDMA, CDMA2000, and Universal Wireless Communications-136 (UWC-136).

The fourth generation (4G) systems may become available even before 3G is fully developed because 3G is a confusing mix of standards. In 4G systems, it is expected that the target data rate will be up to 100-Mbit/sec in pedestrian and 1-Gbit/sec in indoor area possibly higher. 4G will require a channel capacity above 10 times that of 3G systems and must also fully support Internet Protocol (IP) [26]. High data rates are a result of advances in signal processors, new modulation techniques, and smart antennas that can focus signals directly at the users. Orthogonal frequency division multiplexing (OFDM), multiple-input-multiple-output (MIMO), and a combination of the above are promising schemes that can provide extremely high wireless data rates.

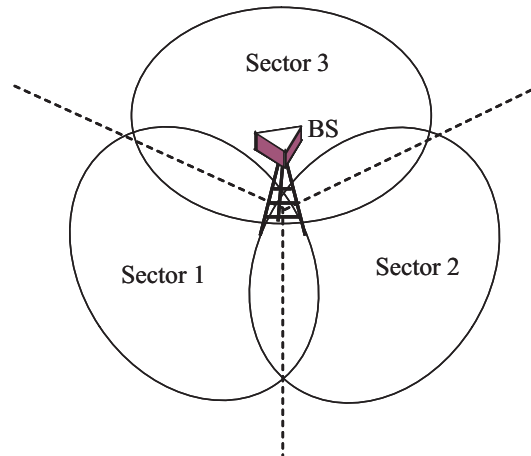


Fig. 1.3: Sector antenna configuration (120-degree beams).

1.3 Smart Antenna Technologies

1.3.1 Overview

The efficient use of the frequency resources is necessary to achieve higher data transmission throughput. Smart antenna systems are capable of automatically changing the directionality of their radiation patterns in response to their signal environment. This can noticeably improve the performance characteristics, such as channel capacity and quality of a wireless system. Smart antenna systems, by using spatially separated antennas, referred to as antenna array, maximize the signal-to-interference-plus-noise ratio (SINR) of the received signals, and suppress interferences and noise power by digital signal processing after analog to digital conversion.

Conventional Antenna Systems

Conventional antenna systems, which employ a single antenna, radiate and receive information equally in all directions. This omni-directional radiation leads to the distribution of energy in all directions. This wasted power becomes a potential source of interference for other users or for other base stations in other cells. Interference and noise reduce the signal-to-noise ratio (SNR) used for detection and demodulation, resulting in poor signal quality. Today's cellular systems usually introduce 120° sectorization of the coverage to enhance capacity and reduce CCI [14]. Figure 1.3 illustrates that three directional antennas can cover each sector area of 120°.

Smart Antenna Systems

On the other hand, smart antennas at the transmitter are capable of steering the maximum radiation pattern toward the desired mobile; at the receiver, they can spatially separate the energy of the interference and mitigate multipath fading using a software algorithm. This ensures that an optimum quality of service is delivered to users, and it provides maximum

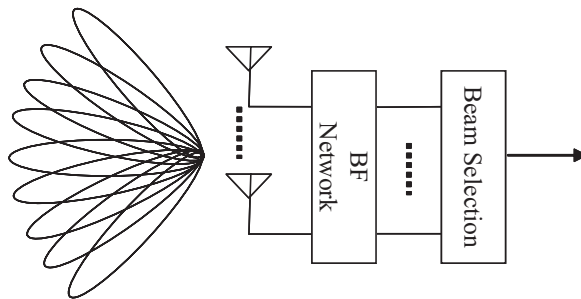


Fig. 1.4: Switched beam antenna configuration.

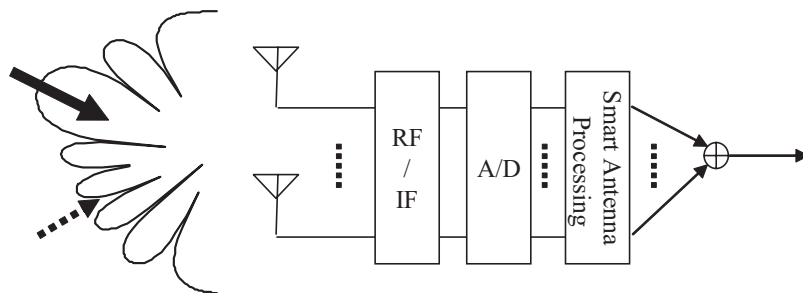


Fig. 1.5: Smart antenna receiver configuration with digital beamforming network.

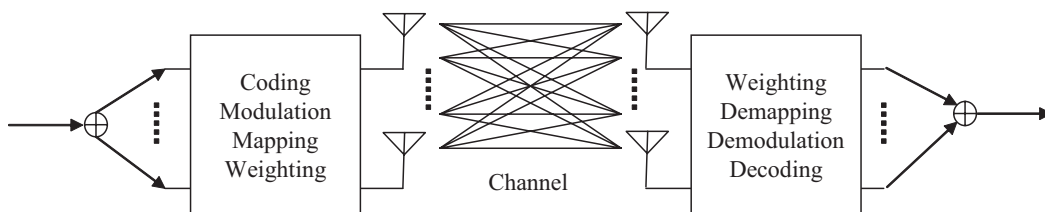


Fig. 1.6: Multiple-Input-Multiple-Output (MIMO) configuration.

coverage for a base station. Smart antennas can use spatial domain processing by using multiple antennas, thus enabling them to have intelligence to process the data at both receiver and transmitter. The smart antennas are often classified as switched-beam arrays and adaptive array antennas [5, 8]. The switched-beam arrays comprise beamforming networks and a beam selection processor, as shown in Fig.1.4. The processor selects the beam with maximum power response by switching the beams. However, the adaptive array antennas incorporate more intelligence than the switched beam arrays. Adaptive array antennas can estimate their environment in accordance with the propagation channel responses between the receiver and the transmitter. This information is then used to weigh the data received at/transmitted from the antenna array to maximize the response for the desired user. Figure 1.5 illustrates the typical configuration of the adaptive array antennas. The processor determines the optimum weight vector for a given environment and thus, the adaptive antennas can combine the received signal maximizing the SINR and not merely SNR. As shown in Figs.1.4 and 1.5, smart antennas can provide space division multiple access (SDMA). In this case, the users may use the same frequency, time, or code allocations over the air interface and only be separated spatially. SDMA can be applied as a complementary scheme to Frequency Division Multiple Access (FDMA), TDMA, and CDMA, thus providing additional capacity enhancement.

MIMO (Multiple-Input Multiple-Output) System

In future wireless systems, both the base station and the mobile station will employ a smart antenna technique, referred to as MIMO system, as shown in Fig.1.6. Ironically, MIMO systems incorporate multipath propagation, which traditionally has been an inherent problem faced by wireless transmission. Multiple spatial channels can be used to dramatically increase the data rate [27, 28]. Moreover, space-time block coding (STBC) techniques have been proposed to improve the channel capacity [29, 30].

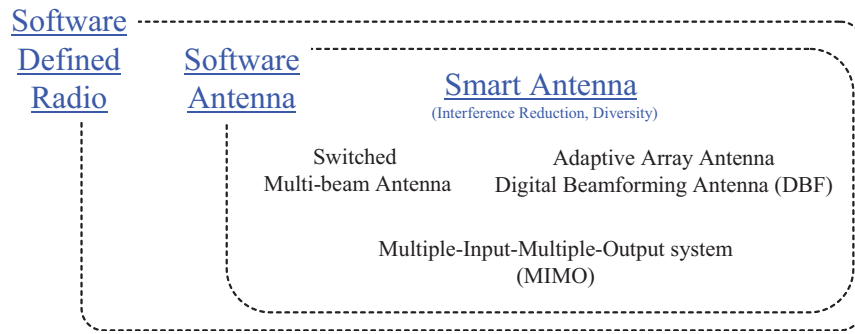


Fig. 1.7: Terminology.

Terminology

In this paper, the term “smart antennas” is used to denote complete antenna systems, including all components from the antenna to baseband digital signal processing. It is often termed “adaptive (array) antenna” [4], “software antenna” [78, 79], or “digital beamforming antenna (DBF antenna)” [9, 10]. Together, these imply an intelligent antenna system different from a conventional omni-directional or fixed-beam antenna system, which merely receive and transmit signals without any adaptive behavior to a change of environment [10, 11, 79]. In [5, 8], the term “smart antennas” is used broadly to imply a multiple antenna system including switched multi-beam antennas and adaptive array antennas. This paper uses the broad term “smart antennas” to imply a similar meaning as “adaptive array antenna”¹. Figure 1.7 shows the relationships between these terms.

1.3.2 Basic Configuration and Optimization Techniques

In general, smart antenna systems consist of the antenna array, frequency converters, data converters, and smart antenna processor, as shown in Fig.1.5. The antenna array is a set of multiple antennas that are designed to receive or transmit the signals with an adaptive beampattern. Arrays have various physical arrangements such as linear, circular, rectangular, etc. The geometry of an array antenna is determined taking into consideration its applications. The primary functions of the Radio Frequency (RF)/Intermediate Frequency (IF) circuitry are frequency conversion, filtering, and amplifying. The critical problem faced in the practical applications of smart antenna systems is the heavy hardware with multiple transceivers and high-performance digital signal processors. However, in order to improve frequency reusability, the smart antenna technology should be integrated in 4G systems.

In order to explain the principle of smart antenna signal processing, the simple discrete wavefront model with narrowband signal is illustrated in Fig.1.8. The array geometry is assumed to be a uniformly equispaced linear array of identical and omni-directional M elements.

¹On the other hand, the term “software defined radio (SDR)” appears to be used in a broader sense. SDR means a set of all target processors required for radio communications, including antenna technology [80]. Hence, “smart antenna” technique might be a part of a SDR technology; however, the terms are often used interchangeably [78].

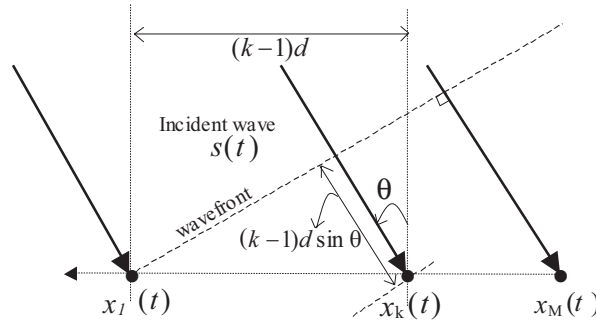


Fig. 1.8: Path difference in planar wave model (linear array of M -element).

The electromagnetic wave arriving at the antenna array is also assumed to be planar. Let the angle between array normal and incident wave be θ ; the far-field expression of the electrical signal at the k -th element at any time t is given by

$$x_k(t) = s(t) \cdot \exp\left(-j\frac{2\pi}{\lambda}d(k-1)\sin\theta\right) + n_k(t) \quad k = 1, 2, \dots, M \quad (1.1)$$

where $s(t)$, λ , and θ are the envelop, wavelength, and direction-of-arrival (DOA) of an incident wave, respectively. $n_k(t)$ is the additive white Gaussian noise (AWGN) at the k -th element, and d is the distance spaced between each antenna. In Eq.(1.1), if $s(t)$ is a narrow band signal, the temporal delay caused by path difference between the elements corresponds to the phase difference. The output of the array antenna is produced by the inner product (multiply-accumulate operation) of input signals and weight coefficients determined by adaptive algorithms as

$$y(t) = \sum_{k=1}^M w_k^* x_k(t). \quad (1.2)$$

Equation (1.2) can be also rewritten by vector expression as

$$y(t) = \mathbf{w}^H \mathbf{x}(t) \quad (1.3)$$

where the superscript H denotes Hermitian transpose operator. The data vector \mathbf{x} is written by

$$\mathbf{x}(t) = \mathbf{a}(\theta)s(t) + \mathbf{n}(t), \quad (1.4)$$

where $\mathbf{a}(\theta)$ denotes array mode vector as

$$\mathbf{a}(\theta) = \left[1, \exp\left(-j\frac{2\pi}{\lambda}d\sin\theta\right), \dots, \exp\left(-j\frac{2\pi}{\lambda}d(M-1)\sin\theta\right)\right]^T, \quad (1.5)$$

In the absence of interference, the adaptive beamforming performs by maximizing the output SNR. In the presence of interferences, the SINR will be maximized by reducing the power of the interference. If a single planar wave arrives through a single path as per the above assumption, Eqs.(1.3)-(1.5) show that the optimum weight vector becomes the mode vector of the incident wave.

However, in an actual multipath propagation environment, the signals arrive in more complex manner experiencing different paths, for example, as

$$\mathbf{x}(t) = \sum_{i=0}^{N-1} \mathbf{v}_i(t, \tau) s_i(t) + \mathbf{n}(t), \quad (1.6)$$

where

$$\mathbf{v}_i(t, \tau) = \sum_{l=0}^{L(t)-1} A_{l,i}(t) e^{j\phi_{l,i}(t)} \mathbf{a}(\theta_{l,i}(t)) \delta(t - \tau_{l,i}(t)), \quad (1.7)$$

$A_{l,i}$, $\phi_{l,i}$, $\tau_{l,i}$, and $\theta_{l,i}$ denote the amplitude, carrier phase shift, time delay, and DOA of the l -th signal component of the i -th mobile, respectively. In general, each of these signal parameters will be time-varying. $L(t)$ is the number of multipath components. The amplitude $A_{l,i}$ of the multipath components is usually modeled as a Rayleigh distributed random variable, while the phase shift $\phi_{l,i}$ is uniformly distributed. The time varying components depend on the Doppler shift f_d [23].

A number of techniques have been proposed to determine the optimum weight, such as minimizing mean square error (MMSE), whose solutions are based on solving Wiener-Hopf equation, maximizing signal to noise ratio (MSN), which is based on generalized eigenvalue problem, and linearly constrained minimum variance filter (LCMV) or directional constrained minimizing power (DCMP), which requires the information of DOAs of desired signals and interferers as *priori*. They require some channel information, such as the training sequence in the case of MMSE and the directional information of incident signals in the case of MSN and LCMV. There are also blind methods, such as constant modulus algorithm (CMA), in which the directional information is not necessary. However, the spatial channel signature such as DOAs of incident signals is often required for efficient spatial domain processing. Various techniques of DOA estimation have been studied as another field of adaptive antenna technologies [7, 12]. We have cited several excellent review papers which report these techniques [5, 7, 13].

1.3.3 Benefits

Smart antennas can provide solutions for three major wireless problems-multipath fading, delay spread, and CCIs-as given below:

Diversity

Smart antennas basically improve SNR with a combination of signals at each branch; additionally, they can provide diversity gain. Diversity technique incorporates the fading uncorrelation. The basic methods by which diversity gain is provided are by using the spatial, polarization, and angle diversity [3]. Among the elements, spatial diversity with spatially separated antennas has a low correlation. Theoretically, among the antenna elements, a M -element smart antenna system has an M -fold diversity gain with sufficiently low fading correlation as well as

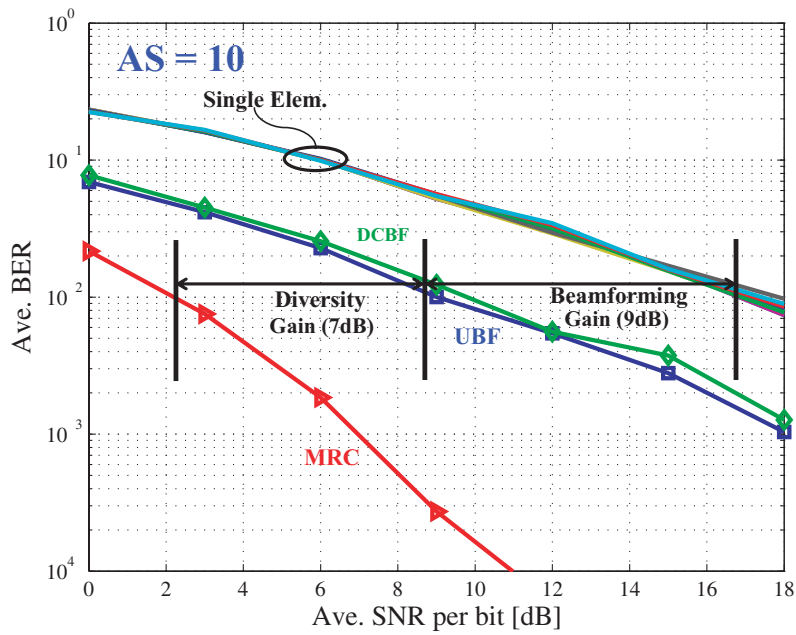
M -fold antenna gain (beamforming gain). When it cancels L interferers ($L < M$), $(M - L)$ -fold diversity gain can be achieved [8]. In an urban cellular basestation, the signals at the base station are received by a scattering process in the vicinity of the mobile station because the antenna is usually deployed higher than the surrounding scatterers. Thus, if the mobile station is sufficiently far from the base station [23], the angle spread (AS) is typically only a few degrees. The measured AS in an urban cellular base station with an antenna height of 35 meters (rooftop of a building) and 80 meters (pylon) at 2 GHz band was reported to be approximately $2 \sim 5$ degrees [25]. Figure 1.9 shows an example of the diversity and beamforming gains in an 8-element antenna array under none-line-of-sight (NLOS) multipath Rayleigh fading channel with an AS of 10 degrees, where UBF, DCBF, and MRC denote the uniform beamformer, Dolph-Chebyshev beamformer, and maximum ratio combiner, respectively. The smaller the AS, the lesser will be the diversity gain achieved, as shown in Fig.1.10, where there is no apparent diversity gain with an AS of 0 degree.

Delay Spread Reduction

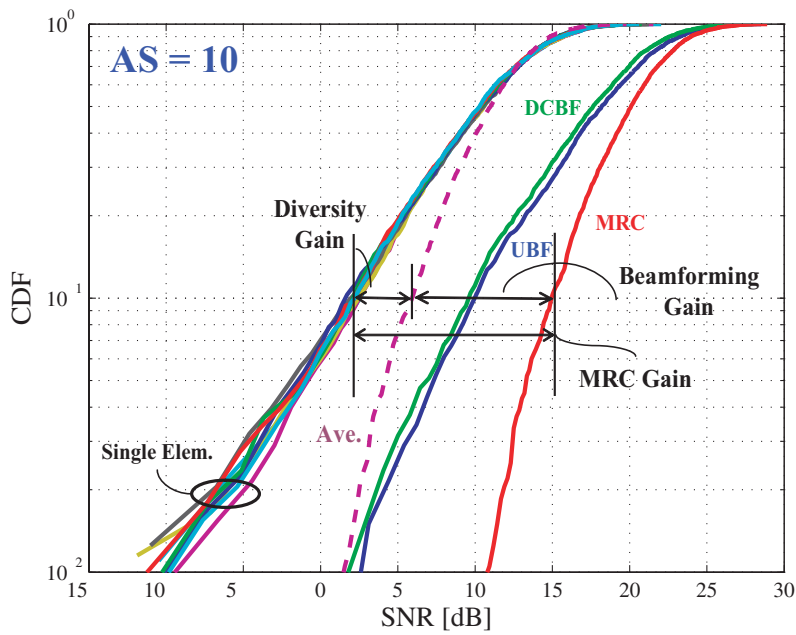
The spatial dimension can be utilized by using multiple antennas in receivers/transmitters. Array signal processing is capable of producing transmit/receive beams toward the desired mobile. It is simultaneously possible to place spatial nulls in the direction of undesired interferences; this is termed as null-steering. This feature can improve the performance of a mobile communication system. Smart antennas have a higher gain than a conventional omnidirectional antenna. The higher gain can be used to either increase the effective coverage, or to increase the receiver sensitivity. Conversely, it can be used to reduce transmit power and electromagnetic radiation in the communication network. Multi-path propagation in mobile radio environments results in ISI. The adverse effects of multi-path and ISI can be reduced by using transmit and receive beams that are directed toward the desired mobile. Smart antenna transmitters emit less interference by only sending RF power that is concentrated in the desired directions.

Interference Suppression

Smart antennas can improve SINR (Signal to Interference and Noise Ratio) performance by adaptively controlling the directivity of the antenna radiation pattern. Interference suppression is enabled by exploiting the spatial dimension; this is not possible with processing in the time domain only. The desired signal and CCI arrive at the receiver with well separated spatial signatures thus allowing the smart antenna to extract the desired signal and suppress the CCIs completely. During transmission, the smart antenna can focus the energy to the desired user, thus reducing the interference for other users.

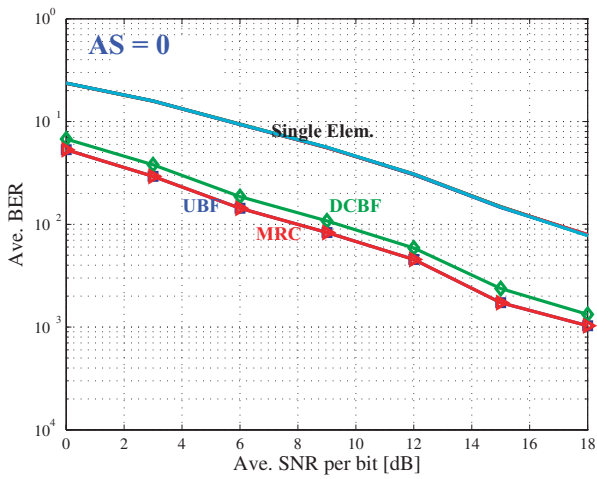


(a) Diversity gain at BER = 0.01

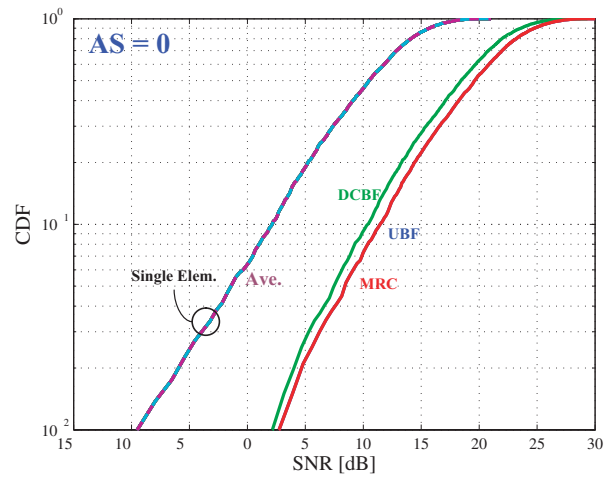


(b) Diversity gain at CDF of output SNR = 0.1% when average SNR = 13 dB

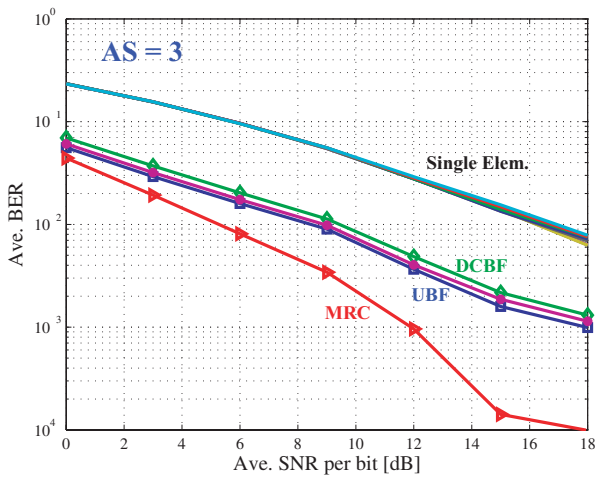
Fig. 1.9: Diversity gains with 8-element antenna array (multipath Rayleigh fading channel, angle spread = 10°).



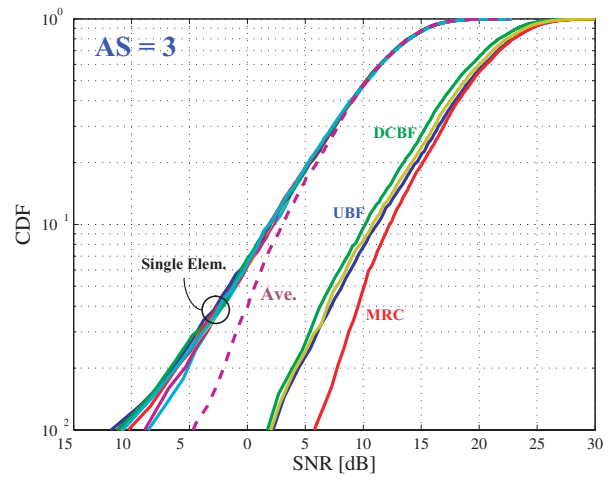
(a) Ave. BER ($AS=0^\circ$)



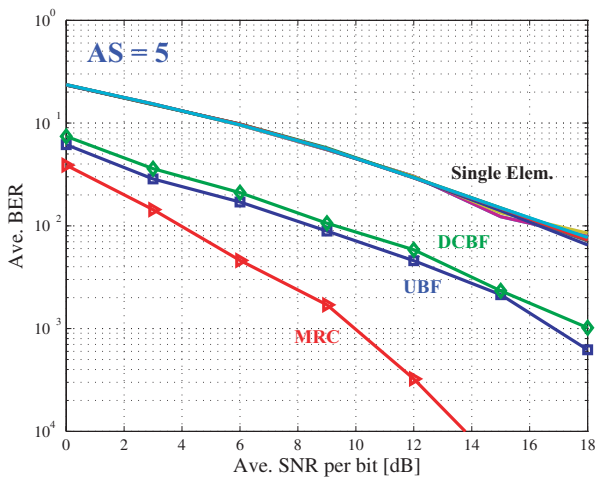
(b) Output SNR ($AS=0^\circ$)



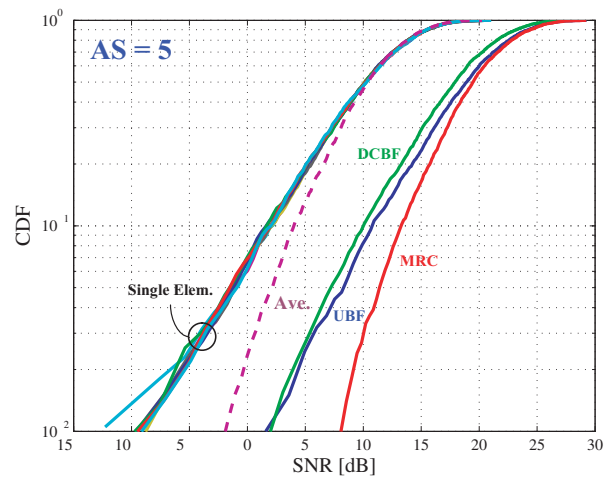
(c) Ave. BER ($AS=3^\circ$)



(d) Output SNR ($AS=3^\circ$)



(e) Ave. BER ($AS=5^\circ$)



(f) Output SNR ($AS=5^\circ$)

Fig. 1.10: Diversity combining with 8-element antenna array (multipath Rayleigh fading channel with small angle spread).

1.4 Smart Antenna System using Direction-of-Arrival Estimation

Smart antennas basically attempt to enhance the desired signal power and suppress the interferers by beamforming toward the DOA of the desired signal and nullsteering in the case of the interferers' DOAs in line-of-sight (LOS) situation. Theoretically, the maximum $(M - 1)$ interferers can be canceled with the M -element array. If LOS exists between the transmitter and the receiver, maximum incident energy is concentrated on the look direction as a single plane wave. The high-resolution estimation techniques for DOAs of incident signals, including Multiple Signal Classification (MUSIC) [31] and Estimation of Signal Parameters Rotational Invariance Technique (ESPRIT) [32], are useful for efficient beamforming. These types of beamforming techniques are based on the angle domain approach that exploits the fading correlation among antenna elements. Hence, diversity gain cannot be achieved.

However, in multipath propagation environments, there may be several situations that are NLOS. In such cases, there are usually a large number of multipath signals, more than the number of antennas. The beamforming in angle domain with DOA information of the propagation channel is not valid here because the DOA of the signal cannot be considered as the single wavefront of a plane wave. However, smart antenna systems can combine the multipath signals and cancel interferences that are less than the number of antenna elements independent of the number of paths in a multipath. On the basis of the signal domain approach, additional diversity gain can be achieved by exploiting the fading uncorrelation among antenna elements. When the delay spread is not sufficiently small, the correlation between the original signal and the delayed versions decreases; thus, the smart antenna system cancels the delayed versions as separate signals. In this case, the supposition that the maximum $(M - 1)$ delayed signals can be canceled with M -element array is also valid [8].

This paper considers a smart antenna system for cellular base station application. As mentioned above, the signals at the base station are received through the scattering process from the local scatterers around the mobile station because the antenna is usually deployed higher than surrounding scatterers, as shown in Fig.1.11. In this case, although the fading across the antenna elements spaced by $\lambda/2$ is highly correlated, the AS is typically only a few degrees. Hence, the angle domain approach exploiting the DOA information can be useful. Moreover, only the DOAs are *commonly* useful channel information in both uplink and downlink channels of Frequency Division Duplex (FDD) systems where each link uses different frequency. This is because the average angular power spectrums in both links are almost identical. Thus, in an uplink, we can estimate the channel parameters with the received data that have passed the channel and apply the estimated DOA information to downlink beamforming. In a downlink channel, smart antenna transmitters can focus the energy to the desired user using the DOA information, and thus reduce the interference for other users. This is the most significant feature of the angle domain approach with DOA estimation.

In fact, the DOA estimation techniques basically assume that the incident waves are planar and incoherent; hence, they are often expressed by discrete wavefronts from point sources. In an urban cellular base station environment, a large number of coherent signals experiencing

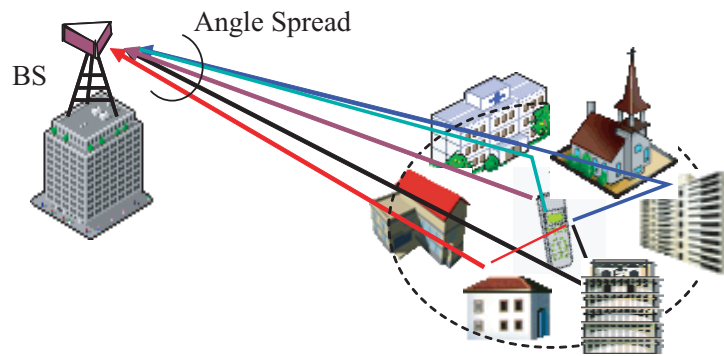


Fig. 1.11: Cellular base station environment for uplink.

multipath of far field local scatterers arrive from spread DOAs. This reduces the fading correlation among the antenna elements. Hence, the SNR at every element becomes a random variable with any distribution and the estimation performance in this case will be degraded [40]. However, various joint estimation techniques of DOAs and AS have been proposed [41–43]. Further, tracking techniques can provide a statistical average performance of DOA estimation in a fading environment with small AS [66]. The main features of the angle domain approach using DOA estimations are as follows:

- Application for urban cellular base station with small angle spread [8, 16].
- Estimated DOAs can be the only common useful information in FDD system [19–21, 66].
- No straight diversity gain; however, angular diversity can be available by combining multipaths [66].
- Large computational load is required for DOA estimation [16].

1.5 Scope and Contributions

This paper aims at the practical and general applications of signal processing implementation of a smart antenna system for wireless cellular basestation systems. While theoretical studies are useful for analyses and simulation purposes, their implementation in real hardware and their validation with actual measurement data will be a meaningful challenge. This paper proposes the smart antenna system based on the DOA estimation of incident signals, which includes fast DOA estimation and beamforming processors. The prototype system integrating signal processors on field programmable gate arrays (FPGAs) was manufactured and the evaluation testbed was configured. The prototype system employs an 8-element antenna array for 5 GHz band and an RF transceiver for each branch. The functionality of the baseband smart antenna processor was verified through hardware simulations and laboratory experiments. The entire hardware system, including RF, antenna arrays, and air interface, at both the transmitter and receiver configurations were also tested in a radio anechoic chamber.

Smart antenna systems, especially those based on DOA estimations, usually require high computational performance for array signal processing. Apart from the hardware complexity of multiple transceivers and an impractically high cost, the limited performance of the signal processing devices has been a big obstacle to its realization. With the general Von Neumann architected processors such as the general micro processing unit (MPU) or the digital signal processor (DSP) with a single or few Multiplier-ACcumulators (MACs), it may be difficult to process a large amount of data from multiple antenna elements in real-time. They also inefficiently consume large power because they are not optimized for the specific purpose. In this paper, FPGAs are basically used as digital signal processors. Due to the recent progress of Very Large Scale Integration (VLSI) technology, FPGAs have evolved from flexible logic design platforms to signal processing engines. FPGAs are now expected to be essential components of a software radio, which includes smart antenna technology, due to their high order of flexibility by SRAM-based structure and real-time processing capabilities. They are inherently suitable for high-speed parallel MAC functions. However, it is incorrect to assume that all DSP functions can always be implemented in FPGAs. Floating point operation is difficult to implement in FPGAs because a large amount of gate resources are wasted and the performance cannot be optimized. Further, processing involving matrix inversion (or scalar division) is also more suitable to a DSP or MPU platform. Therefore, FPGAs and DSP have coexisted for a long time, and a flexible platform usually includes their combination [82].

This paper presents the fixed-point processors of a fast DOA estimator and beamformer implemented with FPGAs. A DOA estimator incorporates unitary MUSIC algorithm, termed “Unitary MUSIC Processor (UMP).” Unitary MUSIC algorithm has a super resolution capability and is suitable for integration on logic circuit devices such as FPGAs. The techniques suitable for FPGAs, such as the eigenvalue decomposition by a cyclic Jacobi processor based on COordinate Rotation DIGital Computer (CORDIC) and spectrum computation by the spatial Discrete Fourier Transformation (DFT), can be exploited to optimize the fixed point arithmetic. This paper also proposes a novel beamforming technique with extremely low complexity that can use the estimated DOA information in the UMP. This beamformer computes the optimum weight vector with a simple convolution operation of precomputed beam and notch patterns; thus, it is able to provide a fast beamforming performance without any matrix inversion in conventional techniques. The major original contributions of this dissertation can be listed at a glance as follows:

- Hardware implementation of smart antenna transceivers testbed.
- Designing a fast eigenvalue decomposition processor based on cyclic Jacobi method with hardware-friendly CORDIC technique [101].
- Fixed-point processor design and simulation of Unitary MUSIC (MULTiple SIGNAL Classification) algorithm [74].
- Hardware implementation on FPGAs of fast DOA estimation processor using Unitary MUSIC algorithm [74].

- Proposal and evaluation of a novel beamforming technique of NDC-BF (Null steering Dolph-Chebyshev beamformer) [49].
- Evaluation of the integrated real-hardware system to verify the functionality.
- Examination of sampling jitter effect on digital downconversion receiver architecture [94].

1.6 Outline

The remainder of this dissertation is organized as shown in Fig.1.12. Chapter 2 introduces the developed hardware platforms of the smart antenna transceiver system and includes its implementation details. The hardware requirements in smart antenna technologies are also discussed. The benefits of FPGAs as array signal processors will be described in comparison with general-purpose DSP processors. The prototype transceivers were designed taking into consideration of the reconfigurable IF processing based on software-defined radio concept as well as the adaptive control of antenna beampattern [78]. In order to implement this, the prototype transceivers are architected by low-IF super heterodyne with undersampling at receivers/harmonic band generation scheme in transmitters. In this chapter, the sampling jitter effect, which determines the maximum IF input frequency, is quantified based on measurements. The implementation of the smart antenna signal processing is described in Chapters 3 and 4. Chapter 3 presents the fast DOA estimation processor using unitary MUSIC algorithm. First, the design of a fast eigenvalue decomposition processor based on a cyclic Jacobi method with the CORDIC technique is described. Second, the implementation of a fast DOA estimation processor termed UMP by FPGAs on a developed transceiver platform is described. The performance will be also quantified by fixed-point hardware level simulation. Chapter 4 proposes a novel beamforming technique with extremely low complexity and presents its performance and hardware implementation. Chapter 5 describes the experimental evaluation of the integrated system performance. The effects caused by real hardware imperfections, such as mutual coupling among antenna branches, are discussed and array calibration issues will be dealt with in this chapter. Finally, Chapter 6 summarizes the dissertation describing the contributions and remaining problems and outlines the future works to be examined.

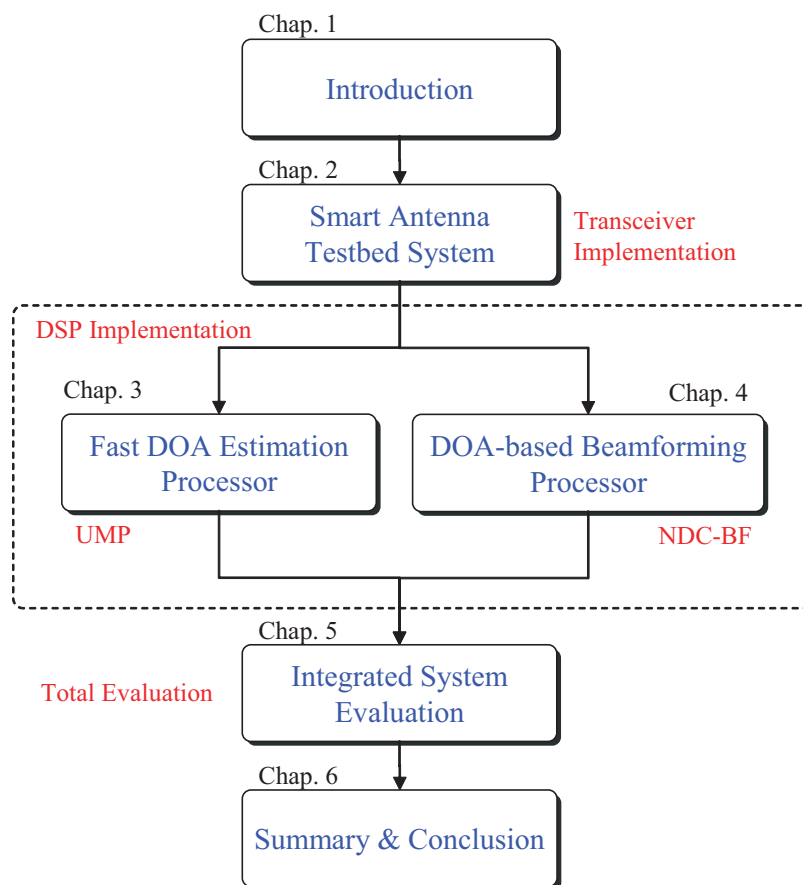


Fig. 1.12: Structure of dissertation.

Chapter 2

Smart Antenna Testbed System

2.1 Introduction

This chapter introduces the developed hardware platforms of the smart antenna transceiver system and its implementation details. First, the hardware requirements to realize smart antenna technologies are discussed from the viewpoint of the SDR concept [80]. The benefits of the FPGAs as array signal processors will be described in comparison with general-purpose DSP processors. This system was designed taking into consideration of the reconfigurable IF processing in accordance with the concept of SDR as well as adaptive control of antenna beampattern [78]. In order to achieve this, a low-IF super heterodyne architecture with under-sampling at the receivers [94] and harmonic band generation scheme at the transmitters [95] is a promising scheme that is currently available. In this chapter, the sampling jitter effect in receivers, which usually determines the maximum IF input frequency of ADCs, is discussed and quantified by measurement. This chapter also introduces the testbed systems involved in RF components and baseband signal processors.

2.2 Hardware Requirements

2.2.1 Digital Transceiver Architecture

Traditional radio transceiver systems perform frequency up/downconversion, mixing, bandpass or lowpass filtering, gain control, and quadrature modulation/demodulation after DACs/before ADCs by analog devices. This section describes smart antenna architecture focusing on the receiver; however, the transmitter is usually completely reciprocal to the receiver. Figure 2.1 shows the traditional super-heterodyne receiver architecture. And, there can be several other receiver architectures as well. On the basis of the number of downconversion stages it has, these architectures are generally classified into direct conversion with only single downconversion stage at RF into baseband and super-heterodyne with more than one downconversion stage at RF into baseband via IF.

However, in a digital radio system, the placement of the ADCs is an extremely critical factor in the entire system architecture. In order to make the systems commercially available and

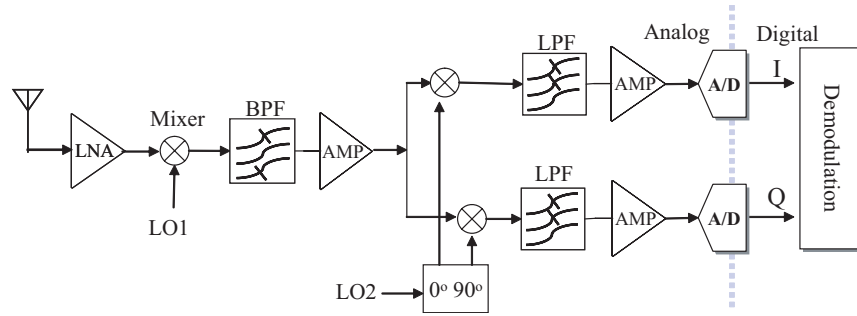


Fig. 2.1: Baseband sampling receiver architecture.

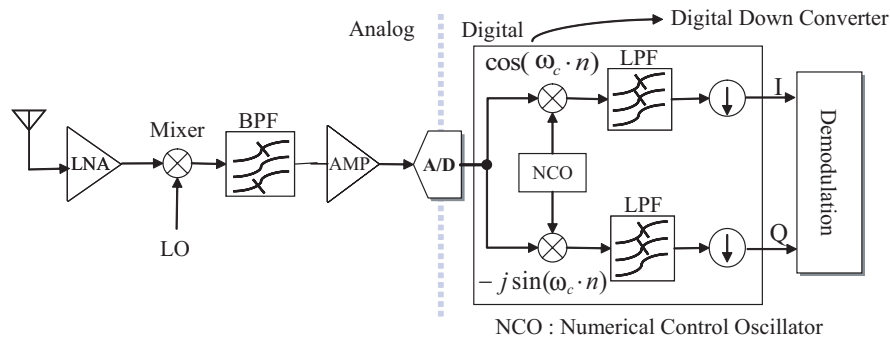


Fig. 2.2: IF sampling receiver architecture.

practically realizable in newer technologies, low IF oversampling architecture is an extremely attractive option. An example of low IF oversampling architecture is illustrated in Fig.2.2. Such a system directly digitizes the downconverted IF signals and subsequently, generates complex baseband signals by the digital downconversion (DDC) function. The DDC consists of a Numerical Controlled Oscillator (NCO), a pair of multipliers (mixers in analog sense), lowpass filters, and decimators for the I and Q component. In this architecture, the analog mixer and lowpass filters are replaced by digital signal processing. The linearity of digital signal processing of mixers and filters ensures the perfect orthogonality of the I/Q signals. In general, once a signal is sampled by an ADC at a high frequency band, fewer analog components are used for downconversion and filtering and the system flexibility will be increased [73].

However, recent technology has provided no easy solution for oversampling the signals directly at the RF or IF band, ranging from tens of MHz to several GHz. For example, the typical sample-and-hold performance of ADCs are degraded with an increase in the input frequency, thus limiting the input frequency bandwidth of ADCs [89]. In addition, more stringent requirements have to be met for extremely high Q analog bandpass filters in order to prevent distortion of the desired signal by strong adjacent channel signals. Currently, there are very few devices that are capable of directly sampling the RF signal; therefore, from the practical and commercial points of view, undersampling is an alternative technique [85].

2.2.2 Data Conversion Devices

The performance of an ADC can be characterized by several parameters. These are resolution, conversion speed, linearity, dynamic range, and power consumption. Usually, the requirement of an ADC depends on its specific application. In SDR technologies including smart antennas, most analog components will be replaced by digital signal processing in order to maximize system flexibility [78, 80]. The digital signal processor can perform various operations including downconversion, demodulation, and filtering. The analog-to-digital converters (ADCs) in such systems will be located as close to the antennas as possible in order to achieve almost complete digital processing. In order to realize this, ADCs capable of digitizing a high-frequency wideband signal at very high sampling rates will be required along with wideband or multi-band antennas and RF analog devices. However, direct analog-to-digital conversion at oversampling rates of very high RF or IF signals, typically ranging between hundreds of MHz to several GHz, may not yet be practical because the reasonably price ADCs and sufficiently high-speed digital devices, such as current signal processors and buffer memories, cannot be used. The undersampling technique is always useful by performing frequency downconversions and quantization at the same time.

2.2.3 Signal Processing Devices

Software radios with smart antenna system implementation lead to a considerable increase in processing requirements. Previously, a single stream of data emanated from a single antenna; now, multiple data streams have to be processed. The data flow in smart antenna processing is not a single-input data stream. We have K data streams that must be processed from the K antenna elements. The basic fundamental operation carried out in a smart antenna system is passing the data stream from each antenna through an adaptive finite impulse response (FIR) filter. It must be noted that in narrowband applications, the adaptive FIR filters simplify to a single weight vector.

If we consider a simple example where we have K ($= 8$ herein) antenna elements and a narrowband system, the computational requirements are

- **Weight computation:** In case of Minimum Mean Square Error (MMSE) smart antenna processing by recursive least square (RLS) method, $4K^2 + 4N + 2$ complex multipliers, or $16K^2 + 16K + 8$ real multipliers per update are required [9, 50]. If 16 iterations are required for the weight convergence per update and the processor serves 8 users every 0.5 ms (2,000 KHz), the total number of real multiply operations required in processing RLS can be obtained by

$$\begin{aligned}
 N_{\text{RLS}} &= r_u (16K^2 + 16K + 8) \quad [\text{ops/sec}] & (2.1) \\
 &= (8 \times 2000 \times 16) \times (16 \times 8^2 + 16 \times 8 + 8) \\
 &= 297 \text{ MOPS}
 \end{aligned}$$

where r_u denotes the update rate (per second) and MOPS stands for mega operation per second. If a real multiplication is approximately equivalent to a floating point operation

in general-purpose processors, 297 MFLOPS (Mega Floating point OperationS) should be required.

- **Beamforming:** Beamforming is performed by the multiplication of the data vectors (multiple data symbols) and the weight vector. For the above condition, the required number of real multiplications is given by

$$\begin{aligned} N_{\text{BF}} &= 4 \times r_b \times L_{\text{frame}} \times K \quad [\text{ops/sec}] \\ &= 4 \times (8 \times 2000) \times 136 \times 8 \\ &= 70 \text{ MOPS} \end{aligned} \quad (2.2)$$

where r_b denotes the beamforming rate that was assumed to be the update rate per 1 ms for 8 users.

- **FIR filtering:** If the receiver employs IF processing such as digital downconversion, which mainly involves FIR filtering, the number of real multiplications required for I and Q components is given by

$$\begin{aligned} N_{\text{FIR}} &= r_s \times n_{\text{tap}} \times (2 \times K) \quad [\text{ops/sec}] \\ &= 40 \times 10^6 \times 8 \times (2 \times 8) \\ &= 5,120 \text{ MOPS} \end{aligned} \quad (2.3)$$

where r_s denotes the sampling rate, which was assumed as 40 MHz and 8-tap FIR filter was assumed.

The resulting amount of processing given above appears to be reasonable for performance by a general-purpose DSP processor that, today, offers approximately 1 GFLOPS. However, if the system needs to support more users and to employ more antennas within a shorter computation time, the processing capability of a general-purpose processor will attain its performance limit. Powerful DSP devices can be developed for handling high-performance requirements by using an application-specific processors, such as Application Specific Integrated Circuits (ASICs) and FPGAs. Furthermore, we can take advantage of the FPGA flexibility for directly handling data acquisition control and other DSP functions such as digital downconversion, demodulation, and smart antenna processing.

FPGAs (Field Programmable Gate Arrays)

Since the VLSI technologies have made significant progress in recent times, the processing speed is increasing and the scale of integration is becoming larger. SRAM-based FPGA technology has led to another alternative solution for digital signal processing. As mentioned above, we can easily have an extremely high-performance DSP processor with multiple MACs using FPGAs. For example, the performance of 1 GOPS (Giga Operation Per Second) can be achieved when 10 MACs operating at 100 MHz are integrated¹. The solution for power consumption is a

¹In a general-purpose DSP, 1 GOPS is equivalent to 1 GFLOPS

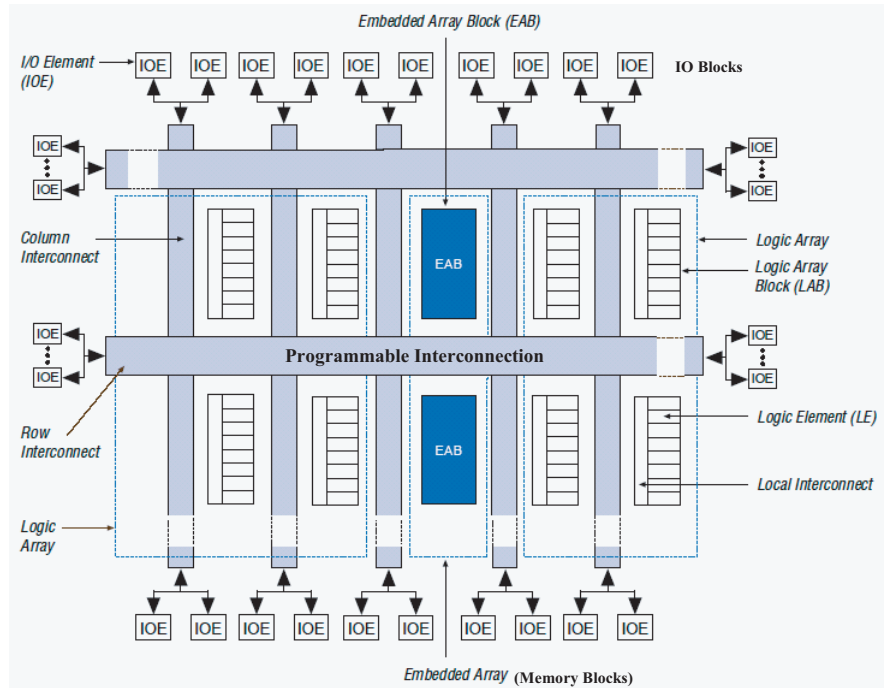


Fig. 2.3: Structure of an SRAM-based FPGA (by Altera Corp.).

significant factor when considering applications for a mobile terminal. FPGA can also provide optimization of power consumption.

A programmable logic device (PLD) is loosely defined as a device with configurable logic and flip-flops (FFs) linked together with a programmable interconnect. An FPGA is a type of programmable logic device that is combined with an array of gates having programmable interconnections with SRAM, logic blocks, and memory blocks, as shown in Fig.2.3. In addition, recent FPGAs often provide dedicated MAC blocks operating at frequencies greater than 200 MHz to meet increasing DSP demands [103]. FPGAs can be reconfigured infinite times after manufacture; however, they are generally distinct from PLDs because they have a higher order of logic capacity. FPGAs consist of logic blocks and an interconnection to connect them. The logic block usually contains lookup tables (LUTs) and FFs store data, as shown in Fig.2.4. Input ports are connected to LUT input ports or FF input ports and outputs from LUTs are either connected to output ports of the logic block or connected to FF input ports. Various combinations of inputs can be chosen by multiplexing, and sequential logic with memory element consisting of FFs as well as combinational logic with LUTs are also available [81].

Digital Signal Processing on FPGAs

There are several methods of implementing digital signal processing. One is to use a general-purpose processor (DSP or MPU), and the other is to use an application-specific device, such as an ASIC. While general-purpose processor solutions are very flexible because their architectures are optimized to process a fixed set of instructions, they may not be ideally suitable for

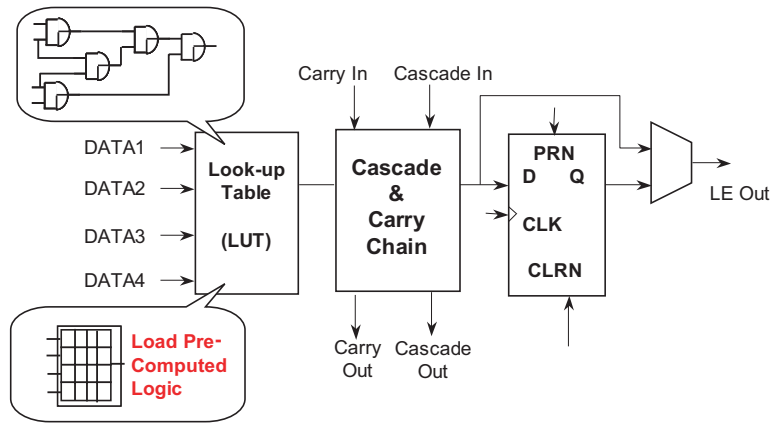


Fig. 2.4: Simple diagram of FPGA logic element (LE) (by Altera Corp.).

the specific application; ASIC solutions enable the designing of a custom architecture that is optimized for a particular application. For example, a general-purpose processor has single or multiple MAC stages so that the computations can be sequentially executed, namely serially. However, an ASIC implementation can have multiple parallel MAC stages. Regarding a specific application, when comparing the performance of the ASIC vis-a-vis the general-purpose processor, it becomes apparent that the latter offers relatively low speed but maximum flexibility (programmability) while the former provides a high speed with minimal flexibility.

On the other hand, an FPGA combines the versatility of a programmable solution with the performance of a dedicated processor, as shown in Fig.2.5. An FPGA can achieve the true aim of parallel processing executing algorithms with the inherent parallelism due to distributed arithmetic structure while avoiding the instruction fetch and data load/store bottlenecks of traditional Von Neumann architectures [62, 63, 81]. Figure 2.6 shows the comparison of MAC operations for an FIR filter in a general-purpose processor with that of a single MAC stage and an FPGA with multiple MAC stages. For example, it can be seen that a 256-tap FIR filter requires 256 iterations of MAC operations in a general-purpose processor while in an FPGA, 256 MACs can operate simultaneously at only one clock cycle. Implementing signal processing function in FPGA devices has the following advantages, as listed in Tab.2.1 [81]. FPGAs are expected to be a key device in the implementation of software defined radios including smart antennas due to their high performance, flexibility, reconfigurability, etc.

FPGAs have evolved from being flexible logic design platforms to signal processing engines. Due to their flexibility and real-time processing capabilities, they are now an essential component of software defined radios, including smart antenna technology. System designers are increasingly porting more and more signal processing functionalities in FPGAs. The flexibility of having the ability to integrate logic design with signal processing is pushing designers to replace traditional DSPs with FPGAs. FPGAs are inherently suited for high-speed parallel multiply and accumulate functions. For example, current generation FPGAs can perform 36×36 MAC operations at speeds greater than 200 MHz. This makes FPGAs an ideal platform for operations such as FFT, FIR filters, digital downconverters (DDC), digital upconverters

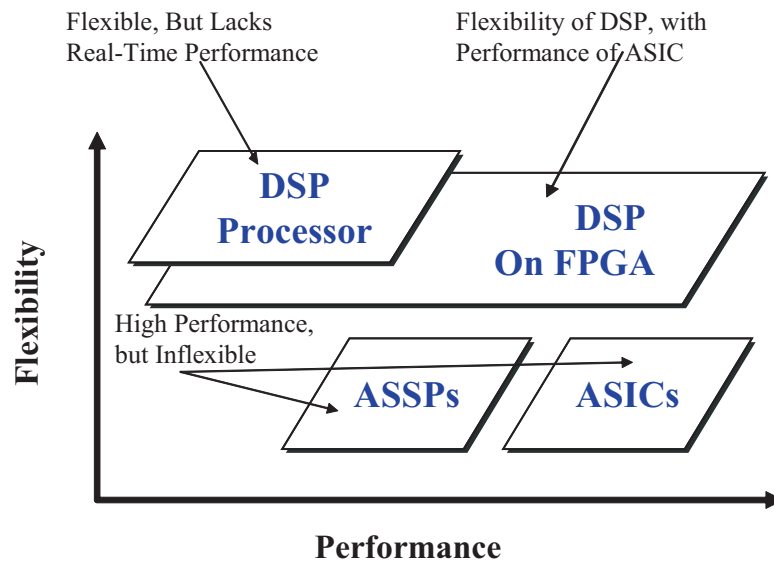


Fig. 2.5: Flexibility vs. Performance (by Altera Corp.).

(DUC), correlators, and pulse compression (for radar processing). However, this does not imply that all digital signal processing functionalities may be implemented in FPGAs. It is difficult to implement floating point operations in FPGAs due to the large amount of area needed in the device. Further, processing involving matrix inversion (or division) is also more suited to a DSP/MPU platform. It can be expected that FPGAs and DSP have thus coexisted for a long time, and a flexible platform will include their combination [82].

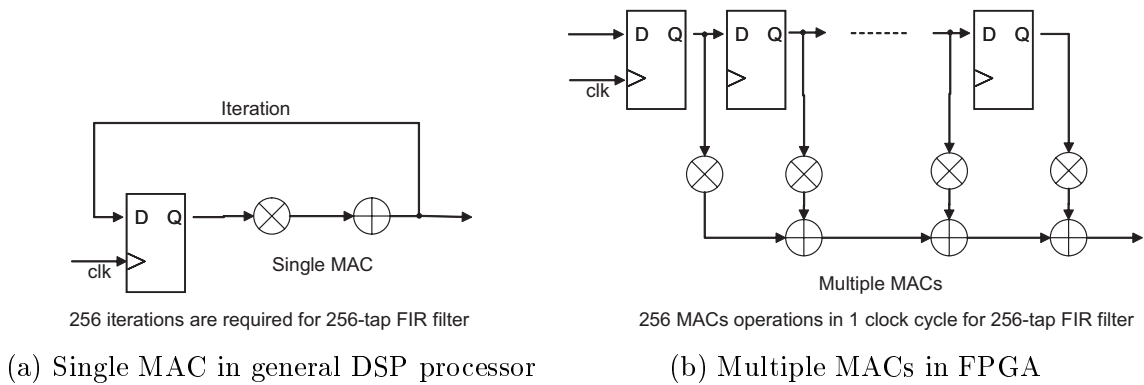


Fig. 2.6: Comparison of MAC operations for FIR filter.

Table 2.1: Comparison of FPGA and DSP processor (simple version of [81]).

	FPGA	DSP
Programmable Languages	VHDL and Verilog	C language and Assembly
Ease of S/W programming	Fairly easy but needs understanding the hardware architecture	Easy
Performance	Very fast if optimized	Speed depends on operating clock speed
Reconfigurability/ Programmability	SRAM-type FPGAs can be reconfigured infinite times	Re-programmable by changing program
Outperforming Area	Digital Filters, FFT, etc	Sequential processing
Power Consumption	Can be minimized if circuit is optimized	Cannot optimize
Implementation Method of MAC	Parallel and distributive arithmetic	Repeat operation of one or a few MACs
Speed of MAC	Can be fast if a parallel algorithm	Depends on operation clock speed
Parallelism	Can be parallelized for high performance	Usually sequential and cannot be parallelized

Table 2.2: Specifications of RF parts.

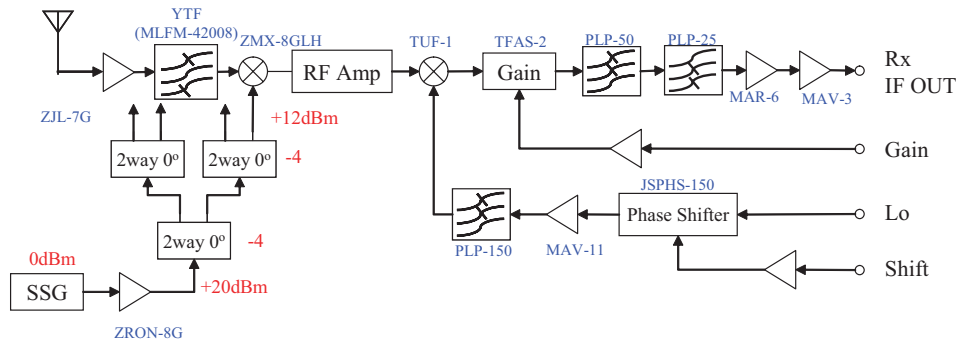
Antennas	8-element sleeve antennas	
Array geometry	Linear array equi-spaced by $\lambda/2$	
RF frequency	2 ~ 5 GHz tunable	
Gain	30 ~ 35 dB	
Bandwidth	20 MHz	
Tx	Channels	4
	IF freq.	1st : 10.7 MHz , 2nd : 160 MHz
Rx	Channels	up to 16
	IF freq.	1st : 160 MHz , 2nd : 40 MHz
	Output volt.	4 V _{pp}
Control	Gain	0 ~ -20 dB
	Phase	$\pm 90^\circ$

2.3 Developed Smart Antenna Testbed System Overview

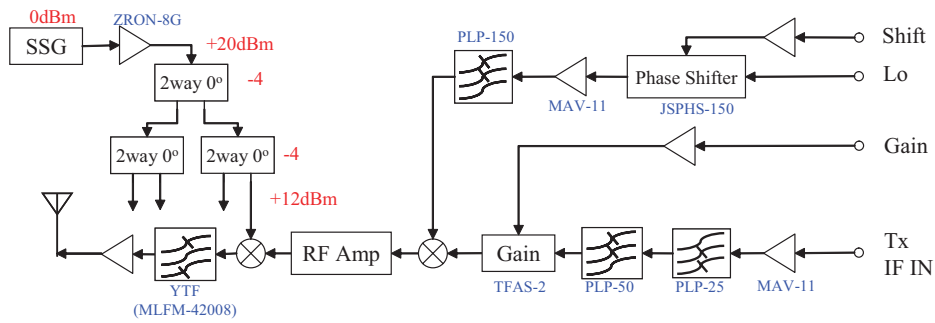
While theoretical studies are useful for analysis and simulation purposes, their implementing on real hardware and validation with actual measurement data will be the meaningful challenge. Certain architectures available for smart antennas were discussed in the previous section from the view point of SDR. We developed a smart antenna testbed system selecting the IF sampling super heterodyne scheme. In this section, the details of the smart antenna testbed systems are described.

2.3.1 Radio Frequency (RF) Components

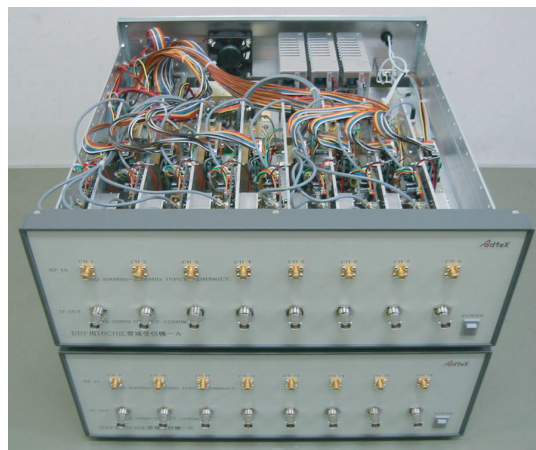
The eight sleeve antennas, linearly spaced by a half wavelength, were used. The RF transceiver configuration is shown in Fig.2.7. It employs Yttrium-Iron-Garnet (YIG) bandpass filters; hence, the RF frequency is tunable from 2 to 5 GHz. In order to achieve an easy phase adjustment at the IF stage, bandpass filters are replaced with a combination of lowpass and highpass filters. The phase and amplitude of the IF output signal can be adjusted by $\pm 90^\circ$ and in the range 0 ~ -20 dB. The IF output frequency at the receiver is 40 MHz and the IF input frequency is 10.7 MHz. The detailed specifications are listed in Tab.2.2.



(a) Receiver Diagram (only 4 CHs depicted.)



(b) Transmitter Diagram (only 4 CHs depicted.)



(c) Photograph

Fig. 2.7: Radio Frequency (RF) transceiver.

2.3.2 Digital Signal Processing Unit

The digital signal processing unit was developed to integrate and evaluate smart antenna signal processors. It consists of the signal processing board and controller board. The signal processing board incorporates 16 channels of ADCs and DACs, and high density FPGAs (approximately 1 mega equiv. gates) for signal processing². A general-purpose CPU (SH4, 200 MHz, HITACH) is used as a system control unit and numerical computation coprocessor with floating-point arithmetic (32 bits). The length of the data bus between the CPU and FPGA is 32 bits. The operating system (OS), NetBSD, is embedded in this system [67]. It also offers a data communication interface via Ethernet. The block diagram of the digital signal processing unit is shown in Fig.2.8 and the photographs are illustrated in Fig.2.9. The data are captured and stored in embedded memory blocks in FPGA where approximately 4 kilowords can be collected for every complex baseband channel with I and Q. The external memory subboard with a SDRAM DIMM module is also available for a large number of continuous samples up to approximately 16 megawords per complex baseband channel of I and Q when using 512 MB SDRAM module. ADCs and DACs have 14-bit resolution and up to 80 MHz and 165 MHz conversion rates, respectively.

Our research group has developed several prototype processing units including the above-mentioned one for a smart antenna testbed system (also see Appendix C) as

- 2-channel receiver processor [68].
- 16-channel receiver and transmitter processors with distributed processing architecture of 4 (data acquisition and IF processing) + 1 (adaptive array processing) FPGAs [69–72].
- 4-channel receiver processor with high performance FPGA (Altera STRATIX) featured by embedded DSP blocks [74].
- 16-channel transceiver processor on single board (current system) [75].

The received RF signals at each antenna element are downconverted into IF. This system performs frequency downconversion again with quasi-coherent detection by digital signal processing. Digital downconversion is a distinguishing feature of the SDR receiver that places ADCs as close to the antenna as possible, digitizes broad band signals and subsequently, performs all functions completely with the software. By replacing the analog IF downconversion stages with digital signal processing, downsizing of system scale, reduction of power consumption, etc. can be achieved. FPGAs are able to perform smart antenna processing with downconverted complex baseband I/Q signals after digital downconversion with quasi-coherent detection.

²In this work, only eight ADC channels were used by the IF sampling scheme. Alternatively, 16 ADC channels can cover an 8-element array with baseband sampling scheme at each channel of I and Q

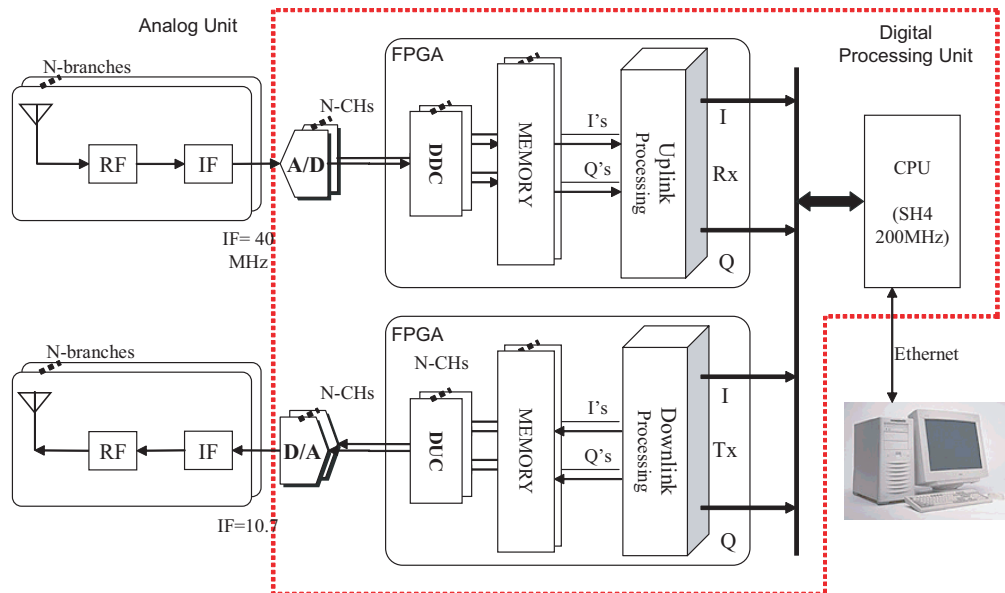
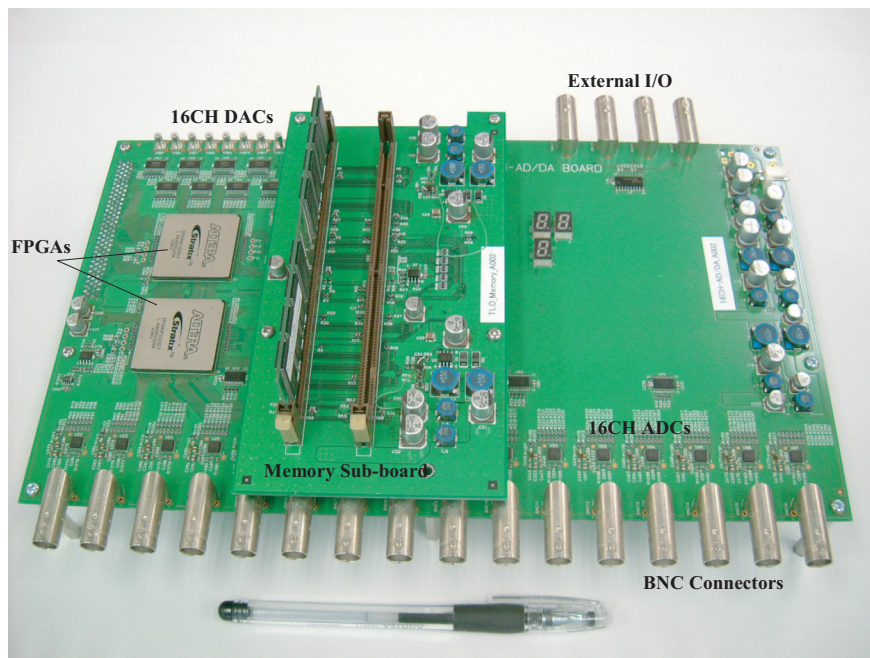
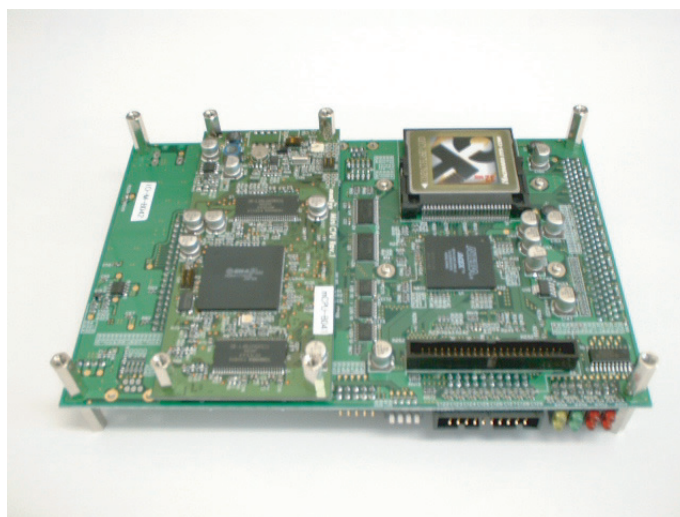


Fig. 2.8: Block diagram of digital processing unit.



(a) Signal processing board including ADCs, DACs and FPGAs.



(b) Controller board (CPU, LAN).

Fig. 2.9: Photographs of digital signal processing parts.

Table 2.3: Specifications of signal processing board.

ADC (Rx)	Part	AD9245 (Analog Device)
	Resolution	14 bits
	Max. sampling rates	80 MHz
	Analog Input BW	500 MHz
	Aperture jitter	0.3 ps (RMS)
	Channels	up to 16
DAC (Tx)	Part	DAC904 (Burrbrown)
	Resolution	14 bits
	Max. data rates	up to 165 MHz
	Channels	up to 16
FPGA	Part	Altera STRATIX EP1S40 \times 2
	LEs	41,250 (1 Mega Gates)
	Embedded Memory	3,423,744 bits
	Embedded DSP multipliers	112 (9 \times 9)
	PLLs	12

Table 2.4: Specifications of CPU board.

CPU	Part	SH4 (HITACHI)
	Operation freq.	200 MHz
	Performance	360 MIPS
OS	NetBSD 1.5	
User I/F	Ethernet 100base-T	

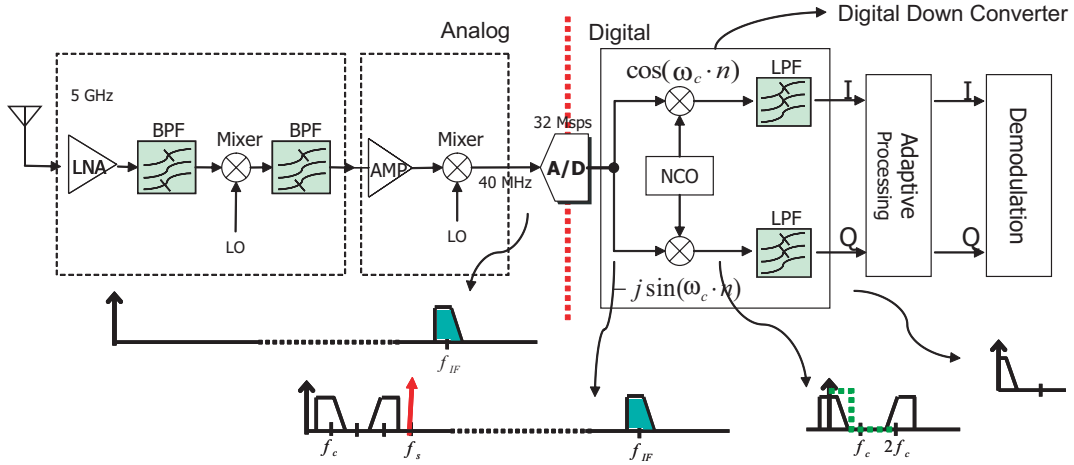


Fig. 2.10: Digital downconverter with quasi coherent detection.

2.3.3 Digital Receiver Implementation

Digital downconversion with quasi-coherent detection can be easily implemented by using NCO, mixer, and lowpass filters, as shown in Fig.2.10. It consists of NCO digital local oscillator and a couple of Finite Impulse Response (FIR) lowpass filters. When digitizing the received analog signals at the IF band, only one ADC is required for each antenna element so that it can reduce the system scale by half when compared with the baseband sampling systems. Bandpass signals can be expressed as a sum of two quadrature components that are $\pi/2$ out of phase. In general, a bandpass signal is represented by

$$x(n) = x_I(n) \cos \omega_c n + x_Q(n) \sin \omega_c n, \quad (2.4)$$

where $x_I(n)$ is the in phase component, $x_Q(n)$ is the quadrature component of the signal $x(n)$, and ω_c is the center frequency of the bandpass signal (carrier frequency). The downconversion process shifts the carrier frequency ω_c to the baseband. It performs a multiplication of the incoming bandpass signal $x(n)$ with the complex phasor $e^{-j\omega_c n} = [\cos \omega_c n - j \sin \omega_c n]$. Subsequently, it lowpass filters the signal of

$$\begin{aligned} \tilde{x}(n) &= x(n) [\cos \omega_c n - j \sin \omega_c n] \\ &= \frac{1}{2} [x_I(n) + x_I(n) \cos 2\omega_c n - j x_I(n) \sin 2\omega_c n \\ &\quad - j x_Q(n) + x_Q(n) \sin 2\omega_c n + j x_Q(n) \cos 2\omega_c n]. \end{aligned} \quad (2.5)$$

The desired frequency shift is accomplished with this operation. After lowpass filtering, the second harmonic components are filtered out and the result remains as the desired complex baseband signal representation of $x(n)$ as

$$\text{LPF}(\tilde{x}(n)) = \frac{1}{2} [x_I(n) - j x_Q(n)] \quad (2.6)$$

[1]. If the sampling frequency is four times the IF center frequency, a combination of the NCO and mixer can be easily implemented. In this system, the combination of NCO and

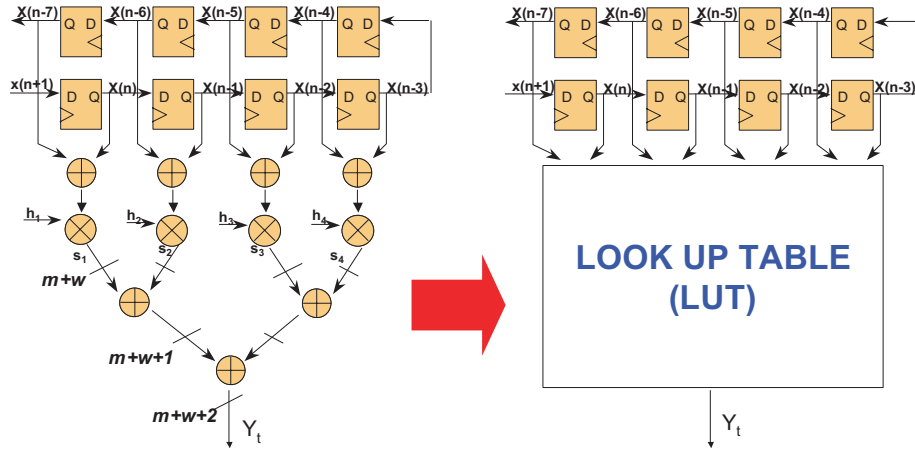


Fig. 2.11: (a) Conventional FIR filter using Symmetry, and (b) FIR Filter using LUT (Look Up Table)

mixer was implemented with a switching circuit in sequential manner of $\{0, x(t), 0, -x(t)\}$. The FIR lowpass filters of 8 taps were used for simplicity.

NCO and Mixer

The downconversion process requires an numerical controlled oscillator (NCO), a mixer multiplying bandpass signal, and a digital local sine/cosine signal generated by NCO as shown in Fig.2.10. There exist various methods by which these can be implemented. Generally, the method of generation of sinusoidal signals by LUT is generally used; however, this system performs downconversion function at a rate of 4 times that of the carrier frequency of bandpass signal. Thus, multiplication-free simple implementation is available.

Lowpass Filter

Digital filter implementation on FPGAs has many advantages over general-purpose DSPs. It is said that a DSP and microprocessor can implement an 8-tap FIR filter at 5 Msps and an off-the-shelf FIR filter at 30 Msps; however, an FPGA can implement an identical filter at over 100 Msps because, as described in the preceding sections, an FPGA is suitable for parallel processing and distributed arithmetic [64]. Digital downconversion requires two of lowpass filters per channel. The inputs are mixed signals of NCO and bandpass signal and the outputs are complex baseband signals of in phase and quadrature. Lowpass filters suppress a second harmonic component and allow only frequency-shifted signals into baseband. In this system, the FIR filter has 8-tap 12-bit registers that are arranged in a shift register configuration. The output of each register, also called a tap, is represented by $x(n)$, where n is the tap number. Each tap is multiplied by filter coefficients $h(n)$, and subsequently, all the products are summed. The equation for this filter is

$$y(n) = \sum_{k=1}^L h(n-k) \cdot x(k), \quad (2.7)$$

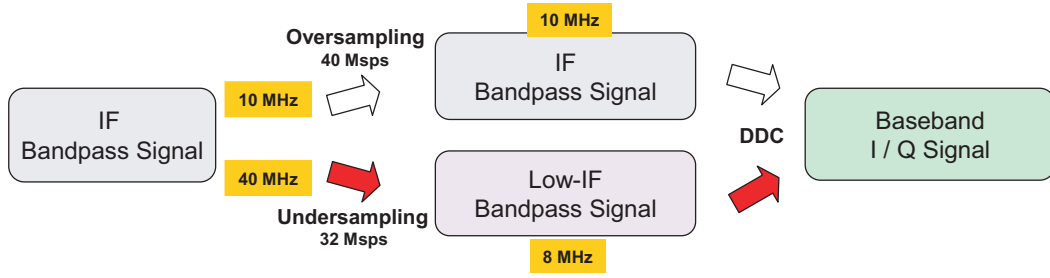


Fig. 2.12: Sampling schemes.

where L is the filter length. In the case of a linear phase response FIR filter, the coefficients are symmetric around the center values. The FIR filter can be reconstructed, as shown in Fig.2.11(a), by taking advantage of the symmetry; this reduces the circuit resource. In addition, Fig.2.11(b) can be optimized by an FPGA using LUTs in a memory block. The multiplication and addition can be performed in parallel using LUTs [64]. As mentioned in the previous section, the recent FPGA technologies can provide high-performance FIR filters using dedicated MAC blocks operating at greater than 200 MHz [103].

Relation of Undersampling and Digital Downconversion

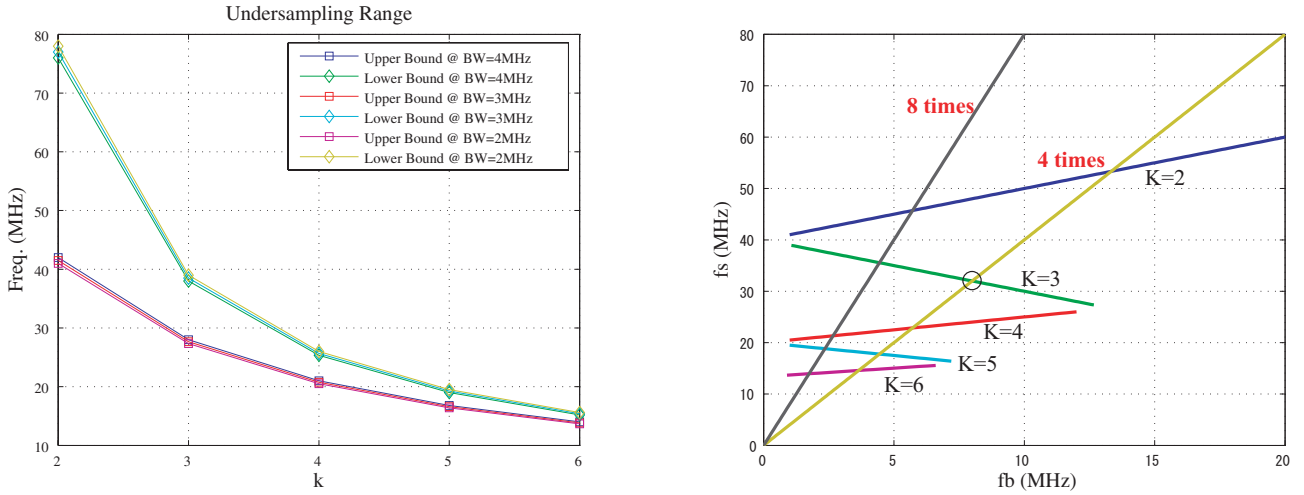
This system was designed by taking into consideration both the sampling schemes of oversampling relatively low frequency signal and the undersampling high frequency signal. Figure 2.12 displays these examples. An IF bandpass signal centered at 10 MHz can be oversampled by an ADC at 40 Msps maintaining the 4 times oversampling rule. As shown in the case of undersampling, the sampling rate of an ADC should be chosen appropriately. In Fig.2.12, 32 Msps is suitable for the IF frequency of 40 MHz. In the case of undersampling, the sampling rate f_s must satisfy the condition as

$$\frac{2f_u}{k} \leq f_s \leq \frac{2f_l}{(k-1)} \quad (2.8)$$

where f_u and f_l is the upper and lower frequency bound, respectively, of an IF signal, and $k (\geq 2)$ is an integer number [83]. Figure 2.13(a) presents the relationships between undersampling range versus k at the bandwidth of 2, 3, and 4 MHz. Further, the 4 times oversampling condition is given by

$$f_s = 4f_b \quad (2.9)$$

where f_b is the in-band signal frequency (downconverted version of input IF signal frequency by undersampling). The above two conditions are plotted in Fig.2.13(b), and the intersections imply that both conditions are satisfied. Tab.2.5 shows the values of the intersections that are shown in Fig.2.13(b). Hence, in this system 32 Msps is typically chosen for undersampling the IF signal at the center frequency of 40 MHz.



(a) Undersampling range.

(b) Undersampling and DDC conditions.

Fig. 2.13: Determination of sampling frequency (IF center freq.=40MHz).

Table 2.5: Candidate sampling frequencies for undersampling of IF signal at 40 MHz.

k	f_s (MHz)
2	53.333
3	32.000
4	22.857
5	17.778
6	14.546

2.4 Undersampling and ADC's Input Frequency Limitation at IF Band

The undersampling (bandpass sampling or subsampling) technique is a useful alternative solution for converting high frequency bandpass signals to lower frequency digital signals exploiting intentional aliasing because of hardware limitations such as data conversion devices and RF analog devices. Traditionally, the sampling rates in an analog-to-digital conversion are determined by Nyquist sampling criterion that specifies the minimum sampling rate required for signal reconstruction. However, in fact, for bandpass signals, the undersampling technique at rates that are more than twice the signal bandwidth can also provide a perfect reconstruction of the original information using in-band aliasing [83,84].

However, the problem is that the dynamic range of ADCs is limited by Signal to Noise Ratio (SNR) degradation that is caused by the sampling jitter effect, which results in amplitude errors. This, eventually, leads to phase errors in the constellation pattern of the phase modulated signals such as Phase Shift Keying (PSK).

We have some research papers including theoretical reviews and mathematical analyses of the jitter effect in analog-to-digital conversion [83–85], as well as certain reports on measurement [86–88]. However, in the communication systems incorporating practical digital downconversion receivers with the undersampling scheme, jitter effects such as Bit Error Rate (BER) and Error Vector Magnitude (EVM) degradation has rarely been reported. This section examines the relationship between the input signal frequency of the ADC and the sampling jitter effect on phase-modulated signals in a digital IF downconversion receiver with undersampling scheme. In order to quantitatively evaluate the jitter effect, we introduced EVM in various clock jitter configurations in the custom testbed system with commonly used and reasonably priced ADCs, the Root Mean Square (RMS) aperture jitter value and sampling rate of which were 0.25 ps and 40 MHz, respectively. The ADC's aperture jitter value is sufficiently small and can be ignored; however, the sampling clock instability is the critical factor in dominating the total jitter condition of the system.

2.4.1 Sampling Jitter Effect in Undersampling Scheme

As mentioned above, the undersampling technique is an extremely useful technique but careful consideration should be taken of the sampling jitter effect caused by the sampling clock instability. This subsection presents the preliminaries of the sampling jitter effect. Further, the problems in a digital downconversion receiver with undersampling scheme are theoretically formulated and some computer simulation results with PSK and Quadrature Amplitude Modulation (QAM) signals are presented.

Sampling jitter is associated with the ADC's aperture jitter due to the uncertainty of the aperture time in the sample-and-hold amplifiers and the sampling clock instability of the system. It results in additional noise power. In reality, it is the sampling clock instability that dominates the sampling jitter condition and not the aperture jitter of ADC itself. As the frequency of the input signal increases, the jitter effect becomes more prominent. Theoretically, the input

frequency of an ADC is limited by the following relation [90] as

$$\frac{dx(t)}{dt} = 2\pi f_{in} A \cos(2\pi f_{in} t) < \frac{\text{LSB}/2}{\sigma_j}, \quad (2.10)$$

where the input signal $x(t)$ is assumed to be full-scale sinusoidal, given by $A \sin(2\pi f_{in} t)$. f_{in} and σ_j are the input IF frequency and RMS aperture jitter, respectively. Since the Least Significant Bit (LSB) $\triangleq 2A/2^M$, the input frequency is limited as

$$f_{in} < \frac{1}{2\pi \cdot 2^M \cdot \sigma_j}, \quad (2.11)$$

where A and M are half of the input range and the resolution of the ADC, respectively. For example, the jitter effect can be completely neglected below approximately 155 MHz, only if the ADC's aperture jitter is taken into consideration, where the aperture jitter and resolution of the ADC are 0.25 ps and 12 bits, respectively. However, the frequency becomes more and more limited due to the sampling clock instability. Assuming that the sampling clock jitter is 100 ps, the input frequency is dramatically limited to below approximately 388 kHz. In other words, the input signals that are higher than the frequency limitation are usually associated with additional jitter noise. The degradation in SNR due to the sampling jitter is typically given by

$$SN_j R \text{ [dB]} = 10 \log \left[\frac{1}{(2\pi f_{in} \sigma_j)^2} \right] \quad (2.12)$$

[87]. Eq.(2.12) also implies that the maximum input frequency is limited by the SNR requirement. In other words, the maximum possible SNR is degraded as the input frequency increases. M. Nagahora et al. have examined the degradation of (Effective Number Of Bits (ENOB), which is proportional to SNR) caused by the sampling clock jitter [88]. They have reported that in order to guarantee an ENOB over 8 bits, the input frequency of the given ADC (AD6640, Analog Devices) was limited to below 50 MHz with a sampling clock jitter of 10 ps.

In the digital receiver system, as shown in Fig.2.2, the downconverted bandpass signal at the IF band is given by

$$r(t) = \text{Re} \left\langle [\hat{s}_{bb}(t)e^{j\varphi} + z_1(t)] e^{j(2\pi f_{cIF}t + \chi)} \right\rangle. \quad (2.13)$$

In Eq.(2.13), $\hat{s}_{bb}(t)$ is the transmitted signal, given by $\sum_k s_{bb}(k) \cdot g(t - kT_0)$, where $s_{bb}(k)$ is the sequence of the data symbols, $g(t)$ is the modulation waveform shaped by filters, and T_0 is the symbol duration [1]. Further, $z_1(t)$ is the complex white Gaussian noise. f_{cIF} , φ and χ are the IF center frequency and the phase offsets due to the propagation delay and initial phase of local oscillators, respectively. After sampling by ADC, IF signals $\tilde{r}(n)$ can be represented by rewriting Eq.(2.13) as

$$\begin{aligned}
\tilde{r}(n) &= r(nT_s + \epsilon(n)) \\
&= \text{Re}\langle [\hat{s}_{bb}(nT_s + \epsilon(n)) e^{j\varphi} + z_1(nT_s + \epsilon(n))] \cdot \\
&\quad e^{j(2\pi f_{cIF}(nT_s + \epsilon(n)) + \chi)} \rangle \\
&= \text{Re}\langle [\hat{s}_{bb}(nT_s + \epsilon(n)) e^{j\varphi} + z_1(nT_s + \epsilon(n))] \cdot \\
&\quad e^{j\left(\frac{2\pi}{N_s}n + J(n) + \chi\right)} \rangle,
\end{aligned} \tag{2.14}$$

where T_s is the sample period and $\epsilon(n)$ is the sampling jitter and the sampling rate

$$f_s \triangleq N_s \cdot f_{cIF}, \tag{2.15}$$

where N_s , an integer, is the oversampling rate of the IF center frequency, and $J(n)$ is the phase variation caused by sampling jitter, given by $2\pi f_{cIF}\epsilon(n)$. The sampled bandpass signal is then multiplied by NCO as

$$\tilde{r}_{bb}(n) = \tilde{r}(n) \cdot e^{j\left\{-\frac{2\pi}{N_s}n\right\}}. \tag{2.16}$$

After the lowpass filtering of Eq.(2.16), the complex baseband signals are obtained as

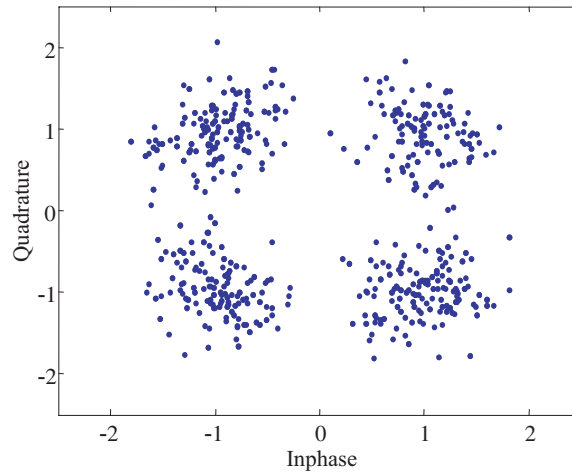
$$r_{bb}(n) = \hat{s}_{bb}(nT_s + \epsilon(n)) \cdot e^{j\{J(n) + \Phi\}} + z_2(n), \tag{2.17}$$

where Φ and $z_2(n)$ are the total phase offset and resulting noise term, respectively. If the symbol period T_0 is considerably larger than the sampling jitter $\epsilon(n)$, the sampling jitter effect on the signal waveform is negligible; thus, Eq.(2.17) is approximated by

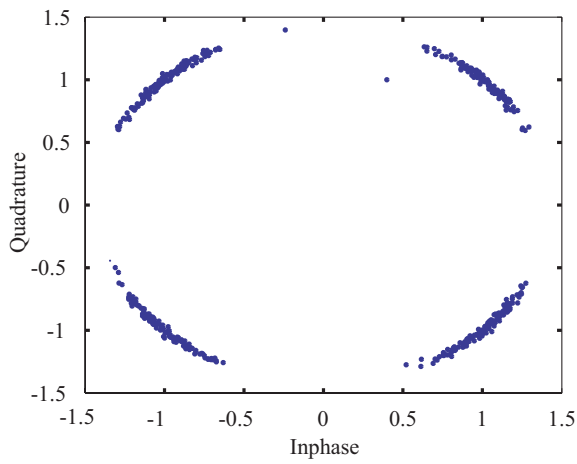
$$r_{bb}(n) \approx \hat{s}_{bb}(n) \cdot e^{j\{J(n) + \Phi\}} + z_2(n). \tag{2.18}$$

From Eq.(2.18), it can be observed that the sampling jitter and the phase offset of local oscillators have effects on the phase error in the constellation pattern of digitally downconverted signals. The phase error $J(n)$ by the sampling jitter becomes larger as the frequency of the input signal increases. Hereafter, this paper assumes that the sampling jitter $\epsilon(n)$ follows the Gaussian distribution of $\mathcal{N}(0, \sigma_j^2)$ and that the variance σ_j has the same meaning as the RMS value of the sampling jitter. Computer simulations confirm the sampling jitter effect on the constellation pattern of Quaternary Phase Shift Keying (QPSK) and 16QAM modulated signals. The oversampling rate N_s of Eq.(2.15) was typically assumed to be four; this makes the multiplication of Numerical Controlled Oscillator (NCO) and the input signal easy to implement by sequentially multiplying $\{1, j, -1, -j\}$ to the input signal. The sampling rate and resolution of the ADC were assumed to be 40 MHz and 12 bits, respectively. The ADC can be obtained at a reasonable price in the today's market. The typical IF center frequency becomes 10 MHz for 4 times oversampling scheme. In this undersampling scheme, the digital downconversion can be applied in an identical manner using the in-band alias at 10 MHz. Herein, the input IF frequencies of ADC were selected as

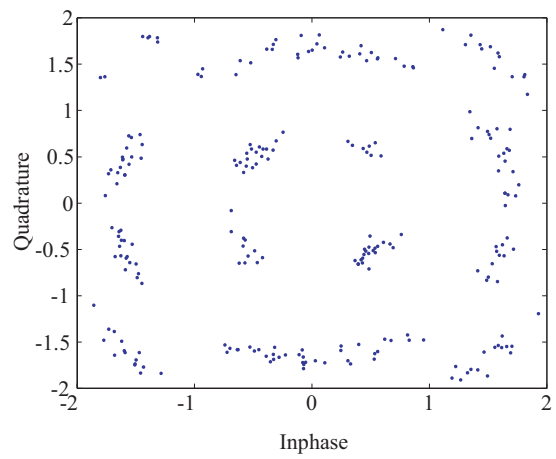
$$\begin{aligned}
f_{cIF} &= 40n + 10 \\
&\begin{cases} n = 0 & \text{(Oversampling)} \\ n = 1, \dots, 8 & \text{(Undersampling)} \end{cases}
\end{aligned} \tag{2.19}$$



(a) Typical constellation pattern
 ($\sigma_j = 25$, $f_c = 170$ MHz, SNR = 7 dB).



(b) QPSK signal
 ($\sigma_j = 150$, $f_c = 170$ MHz, SNR = 30 dB).



(c) 16QAM signal
 ($\sigma_j = 150$, $f_c = 170$ MHz, SNR = 20 dB).

Fig. 2.14: Constellation patterns spread by clock jitter.

Table 2.6: Specifications of jitter measurement system.

IF input Frequency	10 MHz : Nyquist sampling 40 ~ 330 MHz : Undersampling	
ADC	Part	AD9430 (Analog Device)
	Resolution	12 bits
	Sampling rates	40 MHz
	Analog Input BW	700 MHz
	Aperture jitter	0.25 ps (RMS)
FPGA	Altera STRATIX EP1S25 Internal PLL Clock Management	
CPU	HITACHI SH4	
OS	NetBSD	

where f_{cIF} ranged from 40 to 330 MHz.

Figure 2.14(a) shows the constellation pattern of a QPSK modulated signal in practical SNR environments (SNR = 7 dB) in the AWGN (Addictive White Gaussian Noise) channel, where the input signal frequency and the sampling jitter were 170 MHz and 150 ps, respectively. The sampling jitter is so small ($\sigma_j = 25$ ps) that the jitter effect is insignificant because the noise contribution by AWGN is quite dominant. Figure 2.14(b) and (c), however, clearly shows the typical constellation pattern of the QPSK and 16QAM modulated signals spread by the sampling jitter, where the input signal frequency and the sampling jitter were identical to those in the above example. An SNR of 30 dB is sufficiently high to ignore the noise contribution and we observe that the jitter effect appears to be clearer. In fact, the phase errors in the constellation patterns will degrade the BER performance; hence, the sampling jitter effect should be taken into careful consideration in designing the digital IF downconversion receiver with an undersampling scheme.

2.4.2 Evaluation of Jitter Effect

In the case of varying jitter conditions, the jitter effects that were configured in our testbed system are presented. Table 2.6 illustrates the specifications of the testbed system. This system employs a wide-band ADC the analog input bandwidth for which is 700 MHz for undersampling applications [91]. The sampling clock management of ADCs is performed by the FPGA's on-chip internal Phase Lock Loop (PLL). The FPGA's internal PLL is indispensable in designing logic circuits, providing advanced functions of phase shift and frequency manipulation as well as clock lock and boost. However, it has been reported that the sampling clock jitter tends to be enhanced using the PLL [92, 93]. In analog PLLs of Altera FPGAs, nondeterministic noise causes the internal voltage controlled oscillator (VCO) to fluctuate in frequency. The internal control circuitry adjusts the VCO back to the specified frequency; however, this change appears as a clock jitter. Other frequency fluctuations are caused by variations in supply voltage,

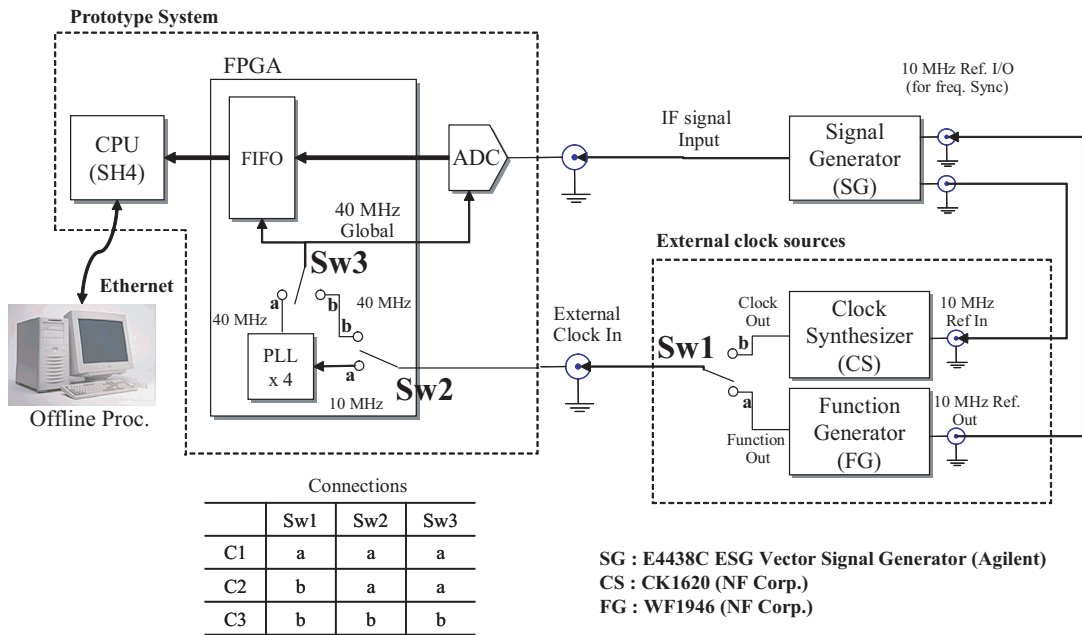


Fig. 2.15: Measurement configuration (clock synchronization network).

Table 2.7: Three different jitter configurations.

Configurations		Estimated RMS Jitters (ps)
C1	Function Generator (FG) + FPGA Internal PLL	150
C2	Clock Synthesizer (CS) + FPGA internal PLL	70
C3	Clock Synthesizer (CS) (Direct clock input)	25

temperature, and a noisy environment [93]. In this testbed system, three jitter configurations were available with different types of sampling clock management; these configurations are illustrated in Table 2.7. **C1** and **C2** used the function generator (FG) and clock synthesizer (CS) as the sampling clock source of 10 MHz, respectively, and the sampling clock was buffered and the frequency was boosted by 4 times in FPGA's internal PLL. **C3** also used the clock synthesizer; however, the clock signal of 40 MHz was directly connected without buffering in PLL. In Fig.2.15, the configurations of the measurement system, including the synchronization network between the equipment, are depicted in detail. Since the general function output from the function generator as a clock source was used, **C1** was considered to be the worst jitter condition. However, the CS used in **C2** and **C3** generates a relatively pure clock signal; thus, the jitter condition was better than that in **C1**. Moreover, **C3** has the best jitter condition

because it is directly connected to ADC's sampling clock pin and does not pass through the FPGA's internal PLL. The jitter values in each configuration were estimated by merely matching the simulation and measurement results of the phase variation with a sinusoidal signal. The RMS jitters in each configuration were estimated as shown in Tab.2.7. The input IF signal was a CW (Continuous Wave) signal generated by the signal generator. The phase variation in the constellation pattern could be easily measured using the CW signal generated by the offline processing of digital downconversion³.

EVM specifications are usually required for many communication system standards. In order to examine the sampling jitter effect on the digital IF downconversion receiver with an undersampling scheme for practical communication systems, the EVM characteristics in each jitter configuration were quantified through the measurements and computer simulations. In addition, the maximum input frequency in such an IF undersampling receiver was discussed. The EVM is obtained by averaging the error vector magnitude as

$$\text{EVM} [\%] = \frac{1}{K} \sum_{k=1}^K \left(\frac{\sum_{l=1}^L |\vec{x}_{p,l}^k - \vec{x}_{0,l}^k|^2}{\sum_{l=1}^L |\vec{x}_{0,l}^k|^2} \right) \times 100 \quad (2.20)$$

where K and L are the number of symbols for the applied modulation scheme and the number of measured points, respectively, $\vec{x}_{0,l}^k$ and $\vec{x}_{p,l}^k$ are the vectors for the ideal point and the practical points of the l -th symbol of k -th frame, respectively. The lowpass filters in the digital downconverter were root-Nyquist filters, and the signal roll-off ratio was 0.5. The coherent detection was taken by each clock synchronization network as shown in Fig.2.15.

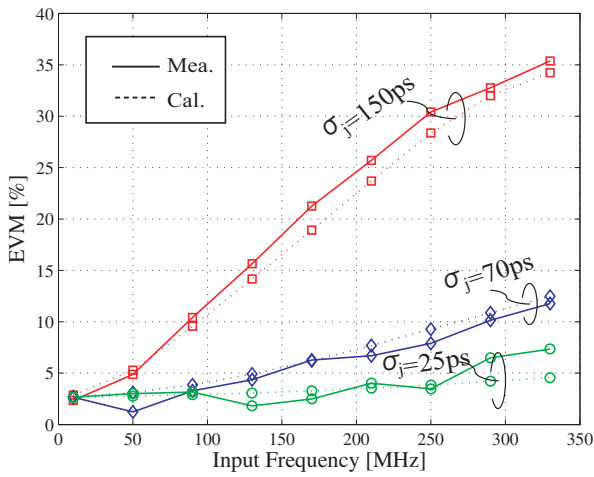
In Fig.2.16(a) and (b), the simulation and measurement results are in relatively good agreement; however, the statistics having more measurements will approximate the simulation results better. The maximum input frequencies for the wireless LAN standard of the EVM below 5% and W-CDMA standard of the EVM below 10% are presented in Tab. 2.8. The results show that in order to meet the specification of the EVM less than 5%, the IF input frequencies f_{cIF} in each jitter condition of $\sigma_j = 25, 70,$ and 150 ps were limited below 290 (210), 130 (50) and 50 (10) MHz, respectively for QPSK (16QAM) signals. Further, in order to meet the specification of the EVM less than 10%, the IF input frequencies f_{cIF} were limited below 730 (450), 250 (170) and 90 (90) MHz, for QPSK (16QAM) signals. It can be clearly observed that the EVM performance is dramatically degraded as the sampling jitter increases.

Additionally, Figs.2.16(c) and (d) show the statistical results of the BER performances of QPSK and 16QAM signals with identical sampling jitter conditions at a given SNR. We determine that the BER performances are further degraded by the additional phase noise caused by the sampling jitter effect in the AWGN channel. We can also quantitatively confirm that the BER performances degrade with an increase in the input frequency.

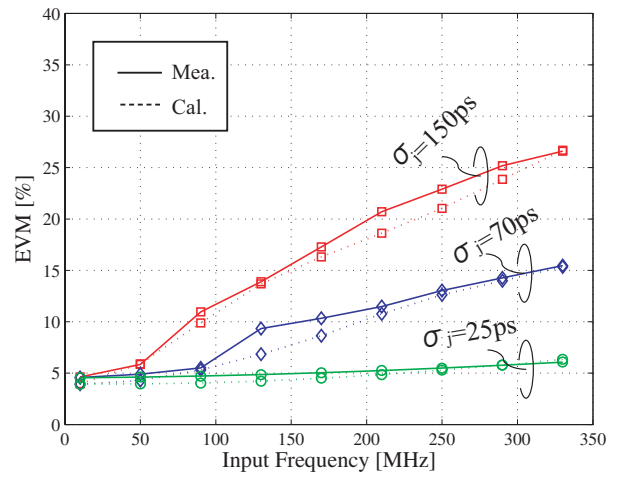
³In fact, the clock jitter can be directly measured by oscilloscopes and estimated by analyzing the measured data.

Table 2.8: IF input frequency limitation.

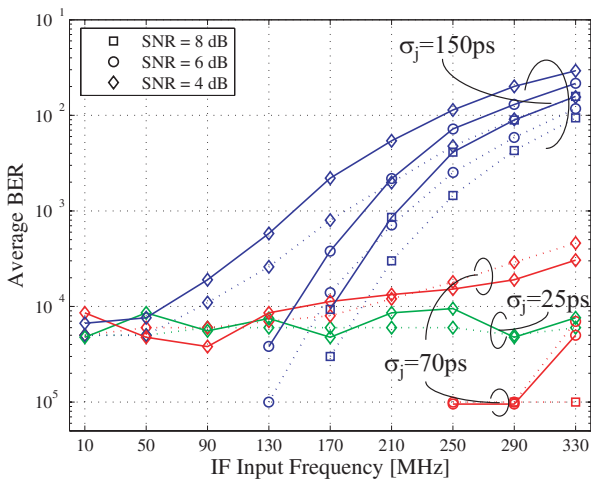
Unit (MHz)	Wireless LAN (EVM < 5%)		W-CDMA (EVM < 10%)	
	QPSK	16QAM	QPSK	16QAM
C1 ($\sigma_j = 25$ ps)	290	210	730	450
C2 ($\sigma_j = 70$ ps)	130	50	250	170
C3 ($\sigma_j = 150$ ps)	50	10	90	90



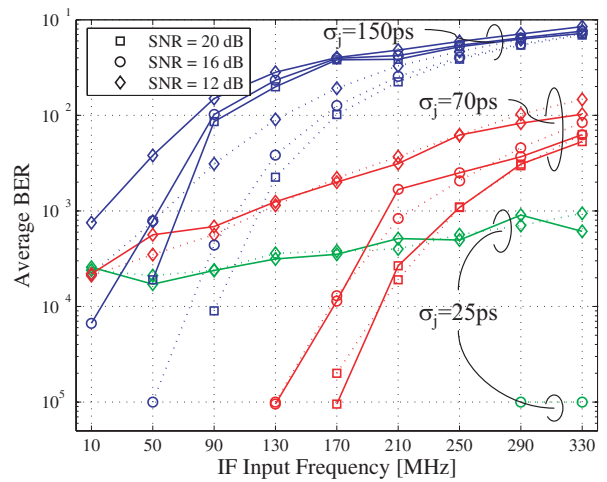
(a) EVM of QPSK signal.



(b) EVM of 16QAM signal.



(c) BER Characteristics of QPSK signal.



(d) BER Characteristics of 16QAM signal.

Fig. 2.16: Jitter effect on EVM and BER.

2.5 Summary

In this chapter, the developed hardware platforms for the smart antenna transceiver system, including its implementation details were introduced. The hardware requirements to realize smart antenna technologies were discussed from the viewpoint of the SDR concept. The benefits of the FPGAs as an array signal processor was described by comparing them with general-purpose DSP processors. The testbed systems involved in RF components and baseband digital signal processors were presented, and the implementation of IF digital processing functions, such as NCO, mixer, and FIR filters, were briefly described. Further, the sampling jitter effect, which usually limits the maximum IF input frequency, was quantified by theoretical analysis and measurement.

Chapter 3

Fast DOA Estimation Processor

3.1 Introduction

DOA information of incoming signals is frequently used in various positioning applications such as emergency systems, radio surveillance system, radar system, military system, etc. In fact, well-known DOA estimation techniques, including MUSIC [31] and ESPRIT [32], basically assume that the incident waves are planar and incoherent; hence, they can be expressed by discrete wavefronts from point sources.

From a theoretical point of view, in smart antenna applications for cellular systems, many excellent smart antenna optimization techniques require the DOAs of the desired signal and interferers in advance [5, 7, 13]. As mentioned in Chapter 1, high-resolution estimation techniques for DOAs of incident signals are useful for efficient beamforming in near line-of-sight (LOS) environments. However, a majority of situations are generally NLOS in multipath propagation environments. In this case, beamforming in the angle domain with DOA information of the propagation channel is not valid because the DOA of the signal cannot be considered as the single wavefront of a plane wave. In general, there exist conventional signal domain approaches of the Minimizing Mean Square Error (MMSE) based combining techniques, such as Least Mean Square (LMS) and Recursive Least Square (RLS). These techniques employ a temporal reference signal instead of the explicit channel information of the DOAs. However, in urban cellular base station environment, the signals at the base station are received through the scattering process in the local scatterers around the mobile station because the antenna is usually deployed higher than the surrounding scatterers. In this case, although the fading across the antenna elements spaced by $\lambda/2$ is highly correlated, and the AS is typically only a few degrees. Thus, the angle domain approach exploiting the DOA information can be useful.

In the case of uplink, we can estimate the channel parameters with the received data that have passed through the channel; however, this is not valid in the case of downlink. In systems, such as Japanese PDC and European GSM, the frequency bands for uplink and downlink are not identical; hence, the small scale fading between uplink and downlink is uncorrelated. However, the DOAs and AS are *statistically reciprocal* in uplink and downlink channels in an FDD system, which use different frequencies at each link. This is the most significant advantage of DOA estimation. Using the knowledge of explicit directional information, the basestations

can steer maximum transmitting power toward the desired user direction. However, DOA estimation is usually a time-consuming task. With the general Von Neumann architected processors, it is be difficult to simultaneously meet the requirements of real-time computation and compact architecture for low power consumption in future communication systems [81].

Although the fast DOA estimator is indispensable for an ideal beamforming with explicit directional information, we have faced several difficulties with regard to its practical high-speed digital signal processor implementation. Some practical studies have been carried out with a dedicated circuit of FPGAs [55]. However, the quantitative evaluation of the fixed-point operation of FPGAs, including the hardware implementation details, has rarely been reported. A recent study implemented a DOA-based smart antenna for European GSM systems using the unitary ESPRIT and Minimum Variance Method (MVM) as DOA estimators [66]. However, it was implemented with a general-purpose processor (DEC Alpha 500 MHz) that may not be optimized for the dedicated tasks and would consume a considerable amount of electrical power.

In this chapter, the digital signal processor of a fast DOA estimator is designed with FPGAs and its hardware implementation is presented. The inherent parallelism, reconfigurability, and optimisability of FPGAs provide more benefits than general-purpose processors. This system will be useful for high speed DOA-based beamforming smart antennas in wireless cellular systems. It incorporates the unitary MUSIC algorithm that is a high resolution DOA estimation technique. When compared with other well-known subspace-based high resolution techniques such as ESPRIT, the MUSIC-like algorithm has many advantages in real hardware implementation due to its simplicity. However, there still remains the computational complication of the arithmetic based on complex numbers, which does not allow for fast computations in the low hardware complexity. Using a unitary transformation, the eigenvalue decomposition (EVD) of the correlation matrix can be solved by computations based only on real numbers [34, 35]. The unitary MUSIC processor (hereafter UMP) performs all digital signal processing procedures only using the fixed-point operation with a finite word-length. The EVD and MUSIC angular spectra computation are solved by a Cyclic Jacobi processor based on fixed-point CORDIC [101] and the spatial DFT, respectively.

3.2 DOA Estimation using MUSIC algorithm

3.2.1 Data Model

Let us assume the basic model of the narrowband signal $s_i(t)$ for the i -th source, where $i = 1, 2, \dots, L$. The signals received at the K -element antenna array spaced by a half wavelength can be modeled by

$$\mathbf{x}(t) = \mathbf{V}\mathbf{s}(t) + \mathbf{n}(t), \quad (3.1)$$

where the array output $\mathbf{x}(t)$ is a snapshot vector, and $\mathbf{s}(t)$ and $\mathbf{n}(t)$ are the signal and complex AWGN vectors, at time t , respectively. The columns of the channel matrix $\mathbf{V} = [\mathbf{v}_1, \mathbf{v}_2, \dots, \text{and } \mathbf{v}_L]$ consist of the spatial channel vectors for L sources. The spatial channel

vector \mathbf{v}_i for the i -th source can be provided by the array response vector \mathbf{a}_i under the assumption that the plane waves arrive at an ideal omni-directional antenna array from the point sources as

$$\begin{aligned}\mathbf{v}_i &= \mathbf{a}(\theta_i) \\ &= \left[1, e^{-j\pi \sin \theta_i}, \dots, e^{-j\pi(K-1) \sin \theta_i} \right]^T,\end{aligned}\quad (3.2)$$

where θ_i is the DOA for the i -th source and the superscript T denotes the transpose operator.

3.2.2 MUSIC algorithm

The MUSIC algorithm is a type of DOA estimation technique based on eigenvalue decomposition (EVD) and it is also called a subspace-based method [31]. It has more advantages, including implementation simplicity and higher resolution, than any other subspace based method. The correlation matrix of $\mathbf{x}(t)$ is given by

$$\mathbf{R}_{xx} = E[\mathbf{x}(t)\mathbf{x}^H(t)] = \mathbf{V}\mathbf{R}_{ss}\mathbf{V}^H + \sigma^2\mathbf{I},\quad (3.3)$$

where $E[\cdot]$ and the superscript H denote the expectation and Hermitian conjugate operators, respectively. Further, $\mathbf{R}_{ss} = E[\mathbf{s}(t)\mathbf{s}^H(t)]$ is the signal covariance matrix and σ^2 represents the noise variance. Since the correlation matrix \mathbf{R}_{xx} is a positive definite Hermitian, it can be decomposed to signal and noise subspaces by the complex-valued EVD as

$$\mathbf{R}_{xx} = \mathbf{U}\mathbf{\Lambda}\mathbf{U}^H,\quad (3.4)$$

where \mathbf{U} is a unitary matrix composed of eigenvectors and $\mathbf{\Lambda}$ is $\text{diag}\{\lambda_1, \lambda_2, \dots, \lambda_K\}$ of real eigenvalues ordered by $\lambda_1 \geq \lambda_2 \geq \dots \geq \lambda_K > 0$. If an eigen vector \mathbf{e}_i is orthogonal to \mathbf{V}^H of rank L , i.e., \mathbf{e}_i is orthogonal to the range of \mathbf{V} , shown by the following relation as

$$\mathcal{N}[\mathbf{V}^H] =^\perp \mathcal{R}[\mathbf{V}],\quad (3.5)$$

then \mathbf{e}_i is an eigenvector of \mathbf{R}_{xx} with the eigenvalue of σ^2 as

$$\mathbf{R}_{xx}\mathbf{e}_i = (\mathbf{V}\mathbf{R}_{ss}\mathbf{V}^H + \sigma^2\mathbf{I})\mathbf{e}_i = \sigma^2\mathbf{e}_i,\quad (3.6)$$

The eigenvectors of \mathbf{R}_{xx} with eigenvalue of σ^2 lie in the nullspace of \mathbf{V}^H . On the other hand, some eigenvectors lie in the range of \mathbf{V} , and the eigenvalues are ordered as

$$\lambda_1 \geq \lambda_2 \geq \dots \geq \lambda_L \geq \lambda_{L+1} = \dots = \lambda_K = \sigma^2.\quad (3.7)$$

They can be partitioned into signal and noise components. In a similar manner, the correlation matrix can be also partitioned as

$$\mathbf{R}_{xx} = \mathbf{U}_s\mathbf{\Lambda}_s\mathbf{U}_s^H + \mathbf{U}_n\mathbf{\Lambda}_n\mathbf{U}_n^H,\quad (3.8)$$

where \mathbf{U}_s and \mathbf{U}_n are the unitary matrices of signal subspace and noise subspace, respectively, and $\mathbf{\Lambda}_s$ and $\mathbf{\Lambda}_n$ are the diagonal matrices of the eigenvalues.

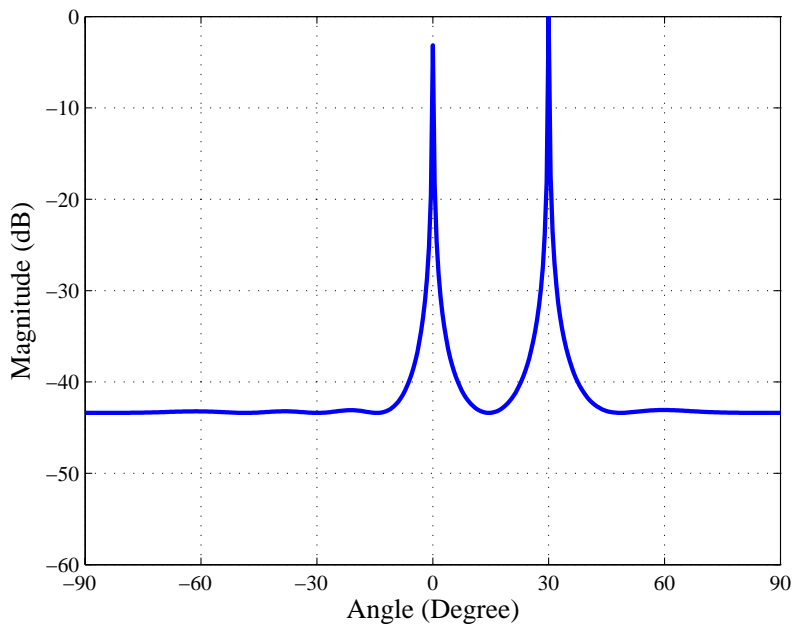


Fig. 3.1: Typical MUSIC spectrum (8-element array, two waves from 0° and 30° with SNR=20dB).

The noise subspace eigenvectors of corresponding eigenvalues of σ^2 are orthogonal to the signal subspace and eventually, orthogonal to the array response vectors. Based on this, the MUSIC spectrum is typically expressed by

$$P_{MU}(\theta) = \frac{\mathbf{a}^H(\theta)\mathbf{a}(\theta)}{\mathbf{a}^H(\theta)\mathbf{E}_n\mathbf{E}_n^H\mathbf{a}(\theta)}, \quad (3.9)$$

where \mathbf{E}_n is the matrix whose columns consist of noise subspace eigenvectors. In the result spectrum of Eq.(3.9), the peaks appear at the DOAs of incident signals. For example, if two incoherent waves are impinging at an 8-element antenna array from $0, 30^\circ$ with SNR = 20 dB and the typical MUSIC spectrum can be calculated, as shown in Fig. 3.1.

3.2.3 Unitary MUSIC DOA Estimation

In reality, the correlation matrix in Eq.(3.3) is complex-valued. It has been clarified that the EVD with a complex-valued correlation matrix would be a high computational burden¹. Reducing the computational complexity by unitary transformation enables real-valued eigenvalue decomposition with the transformed real number correlation matrix [33–36]. Since the EVD procedure bears a large portion of the entire computational load of MUSIC-like subspace based algorithms, real-valued eigenvalue decomposition is a very attractive option to reduce the computation complexity. If the steering vector of Eq.(3.2) is rearranged in the conjugate

¹Generally, complex number multiplication requires four real number multiplications and two real number additions

centro-symmetric manner, the correlation matrix \mathbf{R}_{xx} becomes centro-Hermitian. The real-valued correlation matrix $\hat{\mathbf{R}}_{xx}$ can be obtained by an appropriate unitary transformation \mathbf{Q} as

$$\hat{\mathbf{R}}_{xx} = \text{Re} \{ \mathbf{Q}^H \mathbf{R}_{xx} \mathbf{Q} \}. \quad (3.10)$$

where the unitary transformation matrix \mathbf{Q} for the M -by- M matrix can be chosen as

$$\mathbf{Q} = \frac{1}{\sqrt{2}} \begin{pmatrix} \mathbf{I} & j\mathbf{I} \\ \mathbf{II} & -j\mathbf{II} \end{pmatrix} \quad (3.11)$$

or

$$\mathbf{Q} = \frac{1}{\sqrt{2}} \begin{pmatrix} \mathbf{I} & \mathbf{0} & j\mathbf{I} \\ \mathbf{0}^T & \sqrt{2} & -j\mathbf{0}^T \\ \mathbf{II} & \mathbf{0} & -j\mathbf{II} \end{pmatrix}, \quad (3.12)$$

on the basis of whether the number of antenna elements is even or odd respectively, where the vector $\mathbf{0} = [0, 0, \dots, 0]^T$, and \mathbf{I} and \mathbf{II} are the identity matrix and column flipped identity matrix in the left-right direction, respectively [33, 35, 36].

3.3 Digital Signal Processor Design

The computation flow of the unitary MUSIC DOA estimation involves 4 main steps [34, 101]: (1) estimation of the correlation matrix including unitary transformation and spatial smoothing, if necessary, (2) EVD of the correlation matrix, (3) computation of MUSIC spectrum, and (4) 1-dimensional peak search. This section describes the digital signal processor design for the dominant procedures in a unitary MUSIC DOA estimation algorithm, where we assume that the antenna array has a 4-element linear geometry for simplicity. It is possible to extend the processor using more antenna elements in a different geometry.

The computation flow of DOA estimation by the spectral MUSIC algorithm is illustrated in Fig. 3.2. First, the correlation matrix $\mathbf{R}_{xx}(t)$ is computed by $E[\mathbf{x}(t) \cdot \mathbf{x}^H(t)]$, where $\mathbf{x}(t)$ is the data vector received at the array antenna, $E[\cdot]$ is the expectation operator, and the superscript H denotes the Hermitian conjugate operator. In reality, the average of the correlation matrix with a finite number of snapshots is usually used to approximate the stochastic process. In such a case, the spatial smoothing process decreases the correlation between the incident signals to separate them, although the signals are fully correlated (coherent) with one another. The correlation matrix is decomposed into signal and noise subspace eigenvectors by EVD, and the DOAs can be determined by computing the angular spectrum with an inner product of the noise subspace and the array mode vectors [31].

It appears to be relatively simple to implement the correlation matrix computation, the spatial smoothing filter, and the spectrum synthesis with a dedicated circuit of FPGAs by applying any fast algorithm to them. However, EVD computation, in particular, is rather complex and not suitable for FPGA implementation. In general, the EVD process is believed to have 30 ~ 50% of the entire computational load of the DOA estimation. In fact, there are many algorithms for EVD problems; however, these are merely numerical solutions for serial processing on general-purpose computers with floating-point arithmetic. Therefore, it is necessary to study a hardware-friendly algorithm that is suitable for the parallelism of dedicated circuit, such as FPGAs.

3.3.1 Correlation Matrix with Unitary Transformation

UMP can extract a signal from the correlated mixed signals using the spatial smoothing technique [44]. With the unitary transformation, EVD, which has the largest computational cost among all procedures, can be solved using only real number arithmetic. In addition, the backward averaging effect is obtained by selecting only the real part in Eq.(3.10). Thus, Forward-and-Backward (FB) spatial smoothing can be simultaneously achieved (see Appendix A) [34]. The first step in the unitary MUSIC algorithm is to transform the input data vector \mathbf{x} into \mathbf{y} with a unitary matrix \mathbf{Q} as

$$\mathbf{y}_i = \mathbf{Q}^H \mathbf{x}_i, \quad (3.13)$$

where \mathbf{x}_i and \mathbf{y}_i ($i = 1, \dots, M$) are the divided M sub-vectors of the snapshot vector and the corresponding transformed sub-vectors for spatial smoothing, respectively, as

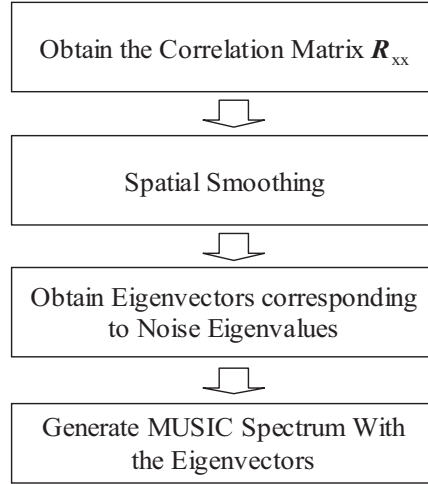


Fig. 3.2: Computational Flow of MUSIC Method

$$\mathbf{x}_i = [x_i, \dots, x_{i+K-M}]^T, \quad (3.14)$$

$$\mathbf{y}_i = [y_i, \dots, y_{i+K-M}]^T. \quad (3.15)$$

By unitary transformation, the real-valued correlation matrix $\hat{\mathbf{R}}_{yy}$ is computed by Eqs.(3.3) and (3.10). In reality, however, it is approximated by uniform averaging with certain numbers of snapshots sampled at time nT , where T is a sampling period, as

$$\hat{\mathbf{R}}_{yy}(n) = \frac{1}{N} \sum_{m=n-N+1}^n \sum_{i=1}^M \text{Re}\{\bar{\mathbf{R}}_{yy,i}(m)\}, \quad (3.16)$$

where

$$\bar{\mathbf{R}}_{yy,i}(m) = \mathbf{y}_i(m)\mathbf{y}_i^H(m), \quad (3.17)$$

and N is the number of snapshots. This type of averaging can be implemented by a sliding boxcar FIR filter with unit gain. In the case of hardware implementation, this filter requires such a long shift register that the memory resources are exhausted. Therefore, the first order IIR (Infinite Impulse Response) exponential averaging filter, as shown in Fig.3.3, is a reasonable choice. It requires only a single register. In this figure, the correlation matrix can be written by

$$\hat{\mathbf{R}}_{yy}(n) = \beta \hat{\mathbf{R}}_{yy}(n-1) + (1-\beta) \sum_{i=1}^M \text{Re}\{\mathbf{y}_i(n)\mathbf{y}_i^H(n)\}, \quad (3.18)$$

where $\beta (< 1)$ is the forgetting factor of a real positive number. This type of filter can quickly respond to the non-stationary channel if the smoothing factor β is determined appropriately².

²In this study, β was typically selected as $0.75(1 - \frac{1}{4})$ or $0.875(1 - \frac{1}{8})$ for easy fixed-point arithmetic with shift and add operation

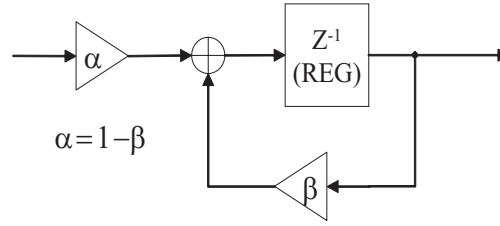


Fig. 3.3: Diagram of exponential averaging filter.

3.3.2 MUSIC Spectrum Computation

After the EVD procedure, the MUSIC spectrum of Eq.(3.9) is computed. In order to reduce the system complexity in the fixed-point system, only the denominator in Eq.(3.9) is considered. This reciprocal spectrum can be generated from the sum of spatial DFT spectra of $(K - L)$ noise eigenvectors, which have been transformed to complex values by the inverse unitary transformation, as

$$P_{\text{MU,reciprocal}} = \sum_{i=L+1}^K |\text{DFT}\{\mathbf{Q} \cdot \mathbf{e}_i\}|^2, \quad (3.19)$$

where \mathbf{e}_i is the i -th eigenvector belonging to the noise subspace.

The angular spectrum in the spectral MUSIC algorithm should be computed in order to determine the DOAs of incoming signals. There exists an alternative solution in MUSIC algorithms; root-MUSIC is based on solving the roots of the MUSIC polynomial, [34,35]. However, the root-determination problem of the polynomial with complex number coefficients is less suitable for the dedicated circuit computer with fixed-point arithmetic, such as FPGAs. A simple iterative algorithm would be best suited for the fast digital signal processor implementation on FPGAs. The spatial DFT technique can be applied to compute the angular MUSIC spectrum. This has a well-known performance guarantee as well as the simplicity of an FFT algorithm. The DFT can be applied to the computation of the MUSIC angular spectrum as follows.

The simple continuous spatial signal model for a 1-dimensional distance is typically given by

$$x_d = u(t) \cdot e^{-j2\pi \cdot f_{\text{spa}} \cdot d}, \quad (3.20)$$

where $u(t)$ includes all the complex-valued time-varying components, and d and f_{spa} are the distance from the first reference antenna element and the spatial frequency, respectively. In the case of array antenna signal processing, we can consider the elements of a snapshot vector as the sampled data at a distance of $m \cdot D_{\text{spacing}}$ in each element of antenna sensors. The distance between each antenna is a discrete value as

$$d \rightarrow m \cdot D_{\text{spacing}}, \quad (3.21)$$

where m and D_{spacing} are the indices of the discrete distance and antenna spacing (or spatial period), respectively. However, the spatial frequency depending on the incident DOA still

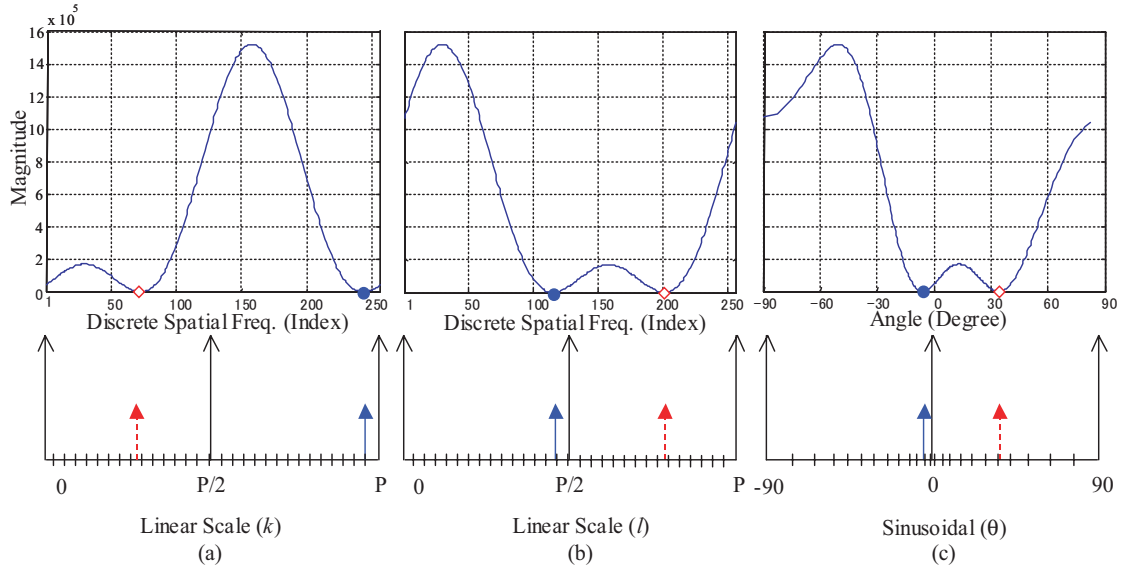


Fig. 3.4: Relationship between DFT indices (k and l) and non-uniform discrete wavefront (θ) in reciprocal MUSIC spectrum ($P = 256$).

remains continuous. Under the plane wave assumption, the continuous spatial frequency can be thought to be P discrete spatial frequencies as

$$2\pi \cdot f_{\text{spa}} \rightarrow \frac{2\pi}{P \cdot D_{\text{spacing}}} k, \quad (3.22)$$

where k is the index of the discrete spatial frequency. Based on this, the discrete spatial frequency domain components can be obtained by applying the spatial P -point DFT as

$$X_d[k] = \frac{1}{P} \sum_{m=0}^{P-1} x_d[m] \cdot e^{-j\frac{2\pi}{P} m \cdot k}, \quad (3.23)$$

when $D_{\text{spacing}} = \lambda/2$. Eventually, the discrete wavefront θ can be computed from the following relationships of Eqs.(3.24)-(3.25).

$$f_{\text{spa,discrete}} = \frac{\sin \theta}{\lambda} = \frac{k}{P \cdot D_{\text{spacing}}} \quad (3.24)$$

$$\theta = \sin^{-1} \left(\frac{k}{P/2} \right) \quad (3.25)$$

From the above facts, it can be observed that in the MUSIC algorithm, the spatial DFTs of the noise subspace eigenvectors in Eq.(3.19) provide the distribution of the spatial frequency. However, the spatial spectrum obtained by DFT with only a few spatial samples as the antenna array length usually has coarse resolution; an accurate estimation is not possible in this case. That is, high-resolution estimation will not be available from the coarse spectrum because the antenna array length is usually limited for practical reasons. Therefore, the interpolation

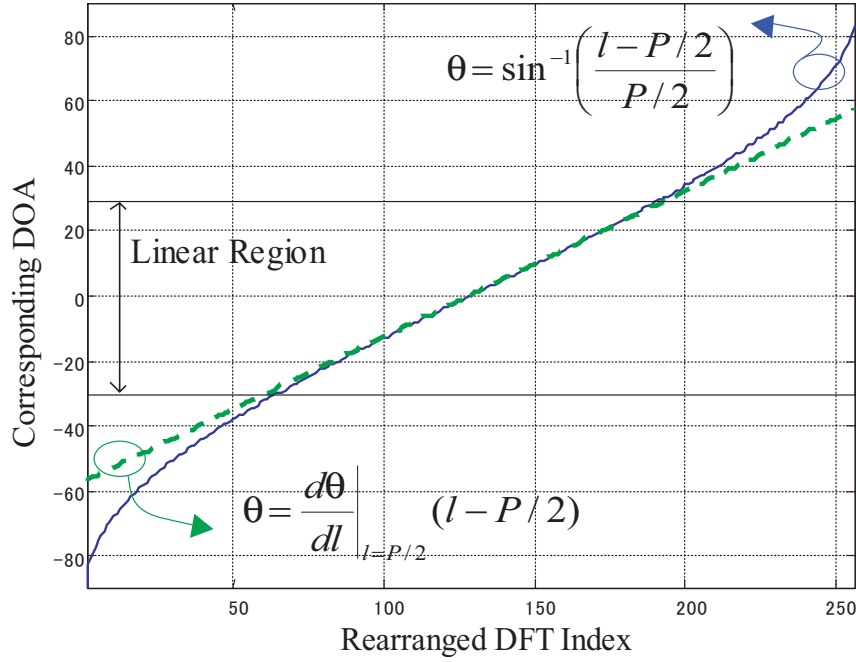


Fig. 3.5: Non-uniform discrete wavefront (DOA) corresponding to DFT index ($P = 256$).

of the spectrum should be considered. According to the digital signal processing theory, the DFT spectrum can be finely and smoothly generated by adding zeroes to the spatial samples of the noise eigenvector elements. The spectrum generated by the spatial DFT is completely equivalent to the denominator of Eq.(3.9)³.

Figure 3.4 shows an example of the relationship among the DFT index k , rearranged index l , and corresponding discrete wavefront θ in the reciprocal MUSIC spectrum (denominator of Eq.(3.9)) generated by spatial DFT (DFT bin $P = 256$). In other words, Fig.3.4(b) is the rearranged version of Fig.3.4(a) (actual order stored in memories) by the relation

$$l = \begin{cases} k + P/2 & (k < P/2) \\ k - P/2 & (k \geq P/2) \end{cases} \quad (3.26)$$

From Eqs.(3.25) and (3.26), the concrete discrete wavefronts (DOAs) in Fig.3.4(c) are obtained as

$$\theta = \sin^{-1} \left(\frac{l - P/2}{P/2} \right). \quad (3.27)$$

As shown in Fig.3.4(c), the discrete wavefronts generated by the spatial DFT spectrum are not uniformly spaced. Thus, the estimation resolution in the angular region close to endfire direction becomes lower as the angular spacing gets wider. However, this can be possibly be neglected in the practical sectorized basestation configuration. According to Eq.(3.27), the DOA θ is an inverse sinusoidal function of l . Figure 3.5 shows the effect of non-uniform

³This implies the angular power spectrum is obtained by scanning main beam toward all directions (P discrete wavefronts).

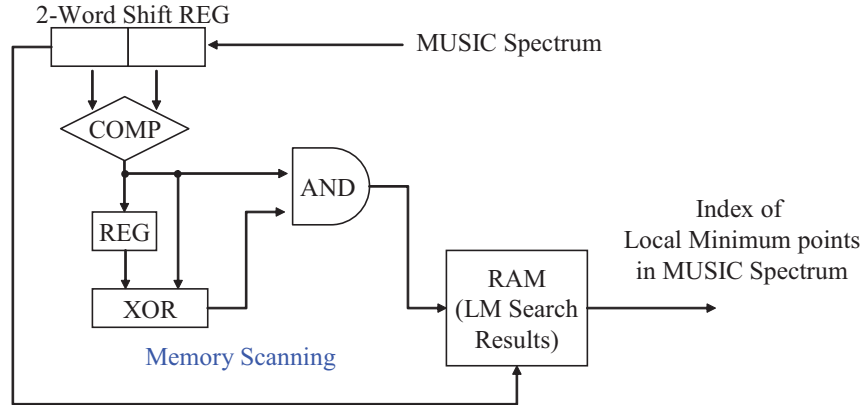


Fig. 3.6: Block diagram of local minima detection.

discrete wavefronts. In the region between approximately -30 and 30 degrees, the estimation resolution can be approximated by a linear function, the gradient of which is given by the derivative of Eq.(3.27) at $l = P/2$ (broadside) as

$$\left. \frac{d\theta}{dl} \right|_{l=P/2} = \frac{1}{P/2} [\text{rad}]. \quad (3.28)$$

In this linear region, the estimation resolution (angular spacing) can be regarded to be almost uniform. Furthermore, the estimation resolution becomes higher with larger P of DFT bin length as that is inversely proportional to P . When P is 256, the estimation resolution is approximately 0.4476° in the linear region from Eq.(3.28).

3.3.3 Local Minima (LM) Detection

Instead of determining peaks in the MUSIC spectrum written in Eq.(3.9), the local minima (LM) detection of the reciprocal MUSIC spectrum generated by DFT in Eq.(3.19) is also available; this enables simple division-free implementation. The LM detection can be implemented by a memory scanning circuit comprising a two-word shift register, comparator, and logic gates of XOR and AND, as shown in the LM detection section of the entire DSP block diagram in Fig.3.6. The comparator compares two words loaded in the shift register to output one-bit decision result $c(n)$ that implies the sign of derivative between the indices $(n-1)$ and n . The AND(\oplus) output of, the $c(n)$ and the XOR(\otimes) output $d(n)$, notifies the memory writing controller of the transition of $c(n)$ ($0 \rightarrow 1$) as

$$\begin{aligned} c(n) &= \begin{cases} 0 & \text{if } s(n-1) > s(n) \\ 1 & \text{otherwise} \end{cases} \\ d(n) &= c(n-1) \otimes c(n) \\ e(n) &= c(n) \oplus d(n). \end{aligned} \quad (3.29)$$

This procedure can be implemented by a simple logic circuit with high-speed operation.

3.4 Eigenvalue Decomposition Processor

In the next step, the correlation matrix is eigen-decomposed by the EVD processor. Generally, the subspace-based methods, such as the MUSIC algorithm, are based on the EVD of the covariance (or correlation) matrix. In the EVD-based system, the complex logic and heavy computational load are usually disadvantages in the real-time processing. This paper proposes a circuit design of a fast EVD processor that is suitable for real-time processing and can be practically used for adaptive antenna processing. It uses the Cyclic Jacobi method that is well known for simple algorithm and easy implementation; however, its convergence time is slower than that of other factorization algorithms such as QR-method [97]. However, if the fast parallel computation of the EVD with a dedicated circuit like FPGAs and ASICs is concerned, the Cyclic Jacobi method can be a suitable choice since it offers a very high degree of parallelism and easier implementation than QR-method [98]. This study uses the hardware-friendly CORDIC algorithm for fixed-point vector rotators and arctangent computers that are the basic processors of this design.

3.4.1 Cyclic Jacobi Method

This section describes the basic principle of the Cyclic Jacobi method, an EVD computation technique. It can be implemented with a simple iterative process of plane rotations. This method solves symmetric eigenvalue problems by applying a sequence of orthonormal rotations to the left and right sides of the target matrix \mathbf{R} ($\in \mathbb{R}^{N \times N}$) as

$$\mathbf{E}^T \cdot \mathbf{R} \cdot \mathbf{E} = \mathbf{D}, \quad (3.30)$$

$$\left(\begin{array}{l} \because \mathbf{E} = \mathbf{J}_1 \cdot \mathbf{J}_2 \cdot \mathbf{J}_3 \cdots, \\ \mathbf{J} = \mathbf{W}_{12} \cdot \mathbf{W}_{13} \cdot \mathbf{W}_{N-1,N} \end{array} \right)$$

where \mathbf{W}_{pq} is an orthonormal plane rotation over an angle θ in the (p, q) plane, whose elements are $w_{pp} = \cos \theta$, $w_{pq} = \sin \theta$, $w_{qp} = -\sin \theta$, and $w_{qq} = \cos \theta$ ($p > q$), and is defined as Eq.(3.2). \mathbf{J} is the multiple rotation of \mathbf{W}_{pq} 's in the cyclic-by-row manner of (p, q) , which is termed a Jacobi sweep; the superscript T and N denote the transposition operator and array length, respectively.

$$\mathbf{W}_{pq} = \begin{pmatrix} 1 & & & & & & & & \\ & \ddots & & & & & & & \\ & & \cos \theta & \cdots & \sin \theta & & & & \\ & & \vdots & 1 & \vdots & & & & \\ & & -\sin \theta & \cdots & \cos \theta & & & & \\ & & & & & \ddots & & & \\ & & & & & & & & 1 \end{pmatrix} \quad (3.31)$$

Theoretically, it is certain from the infinite number of transformation of the matrix \mathbf{R} that \mathbf{E} and \mathbf{D} converge into the matrix, whose column vectors are composed of eigenvectors and

the matrix, whose diagonal elements are eigenvalues. A symmetric matrix \mathbf{R} is transformed to \mathbf{R}' by plane rotation as

$$\begin{aligned} \mathbf{R}' &= \mathbf{W}_{pq}^T \cdot \mathbf{R} \cdot \mathbf{W}_{pq} \\ &= \begin{pmatrix} \cdots & r'_{1p} & \cdots & r'_{1q} & \cdots & \\ \vdots & \vdots & & \vdots & & \vdots \\ r'_{p1} & \cdots & r'_{pp} & \cdots & r'_{pq} & \cdots & r'_{pN} \\ \vdots & & \vdots & & \vdots & & \vdots \\ r'_{q1} & \cdots & r'_{qp} & \cdots & r'_{qq} & \cdots & r'_{qN} \\ \vdots & & \vdots & & \vdots & & \vdots \\ \cdots & r'_{Np} & \cdots & r'_{Nq} & \cdots & & \end{pmatrix}. \end{aligned} \quad (3.32)$$

By the above transformation, only the p -th and q -th rows and columns of \mathbf{R}' are changed as Eq.(3.32). The optimal rotation angle in a (p, q) plane is determined by Eq.(3.33). The basic strategy of the Cyclic Jacobi method is that the iterative process of the plane rotation converges the (p, q) and (q, p) elements of the target matrix into zero.

$$r'_{pq} = r'_{qp} = 0 \quad (3.33)$$

In a similar manner as described above, matrix \mathbf{R} converges into a diagonal eigenvalue matrix. In the Cyclic Jacobi method, the off-diagonal quantity $S^{(h)}$ is defined by

$$S^{(h)} = \sqrt{\frac{1}{2} \left[\|\mathbf{R}^{(h)}\|_F^2 - \sum_{i=1}^N \{r_{ii}^{(h)}\}^2 \right]}, \quad (3.34)$$

where $\|\cdot\|_F$ denotes the Frobenius norm. Therefore, if $S^{(h)}$ converges into zero, the target matrix \mathbf{R} becomes the eigenvalue diagonal matrix as

$$\lim_{h \rightarrow \infty} S^{(h)} \rightarrow 0 \Leftrightarrow \lim_{h \rightarrow \infty} \mathbf{R}^{(h)} \rightarrow \text{diag}[\lambda_1, \cdots, \lambda_N]. \quad (3.35)$$

On the other hand, the execution of a similarity transformation yields

$$\left[S^{(h+1)} \right]^2 = \left[S^{(h)} \right]^2 - \left[\{r_{pq}^{(h)}\}^2 - \{r_{pq}^{(h+1)}\}^2 \right]. \quad (3.36)$$

From Eq.(3.36), the maximal reduction of $S^{(h)}$ is obviously obtained if $r_{pq}^{(h+1)} = 0$. The condition for an optimal angle and maximal reduction of $S^{(h)}$, is achieved as

$$\theta_{opt} = \frac{1}{2} \tan^{-1} \left[\frac{2r_{pq}}{r_{pp} - r_{qq}} \right] = \frac{1}{2} \tan^{-1} \tau, \quad (3.37)$$

where $\tau = \frac{2r_{pq}}{r_{pp} - r_{qq}}$ [97, 98].

3.4.2 CORDIC Algorithm

The CORDIC algorithm is operated in one of two modes?rotation mode and vectoring mode [99]. In this study, the rotation mode is used for fixed-point vector rotations and the vectoring

mode is used for computing the optimal rotation angle by arctangent of τ . In the case of the rotation mode, the CORDIC equations are

$$\begin{cases} x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i}) \\ d_i = -1 \text{ if } z_i < 0, \text{ } +1 \text{ otherwise} \end{cases}, \quad (3.38)$$

where $d_i = \pm 1$ (direction of rotation) and z is the angle accumulator. The CORDIC algorithm provides the following results after a finite number of iterations that is as many as the word length.

$$\begin{aligned} x_n &= A_n (x_0 \cos z_0 - y_0 \sin z_0) \\ y_n &= A_n (y_0 \cos z_0 + x_0 \sin z_0) \\ z_n &= 0 \\ A_n &= \prod_{i=0}^n \sqrt{1 + 2^{-2i}} \end{aligned}, \quad (3.39)$$

where A_n is a computational gain.

On the other hand, the CORDIC equations for the vectoring mode are

$$\begin{cases} x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i}) \\ d_i = +1 \text{ if } y_i < 0, \text{ } -1 \text{ otherwise} \end{cases}, \quad (3.40)$$

which also provides the following result after a finite number of iterations, as

$$\begin{aligned} x_n &= A_n \sqrt{x_0^2 + y_0^2} \\ y_n &= 0 \\ z_n &= z_0 + \tan^{-1}(y_0/x_0) \\ A_n &= \prod_{i=0}^n \sqrt{1 + 2^{-2i}} \end{aligned}. \quad (3.41)$$

After the final step, scaling operation must be performed elsewhere in the system. From Eqs.(3.39) and (3.41), the scaling factor K_n is obtained by

$$K_n = \frac{1}{A_n} = \prod_{i=0}^n \frac{1}{\sqrt{1 + 2^{-2i}}}; \text{ Scaling factor.} \quad (3.42)$$

Due to the use of 2^0 for the tangent in the first iteration, the rotation and vectoring modes of CORDIC algorithm are usually restricted to rotation angles between $-\pi/2$ and $\pi/2$.

Circuit Architecture

The CORDIC algorithm performs only shift and add operations; hence, it is easy to implement and suitable for dedicated circuit in a fixed-point system. In the implementation of the CORDIC algorithm, we can choose various designs depending on what is given greater importance?circuit resource or performance. CORDIC algorithm can be implemented by bit-serial

or bit-parallel, and unrolled or rolled (iterative) architectures [61]. This study uses the bit-parallel unrolled CORDIC architecture for high performance. It is a cascade structure of the consecutive CORDIC stages, as shown in Fig.3.7, where arctangent values are precomputed and stored in any memory block.

Arctangent Computer

If the angle accumulator z is initialized with zero ($z_0 = 0$), the arctangent, $\theta = \tan^{-1}(y/x)$, is directly computed using the vectoring mode. The result is taken from the angle accumulator as

$$z_n = z_0 + \tan^{-1}(y_0/x_0), \quad (3.43)$$

[61].

Scaling in Double Rotation Architecture

In CORDIC processing, scaling must be performed to avoid overflow caused by the finite word-length of the fixed-point processor. However, as is seen from Eq.(3.42), the scaling and normalizing operations using pre-computed scaling values cannot be performed only with shift and add operations. It may not be easy to implement the division and square root operation in a fixed-point system.

Double rotation by $z_0/2$ can solve this problem [98]. Let an elementary rotation by angle z_0 be composed of double rotation by $z_0/2$. Hence, Eq.(3.38) is rewritten as

$$\begin{cases} x_{i+1} &= (1 - 2^{-2i})x_i - y_i \cdot d_i \cdot 2^{-i+1} \\ y_{i+1} &= (1 - 2^{-2i})y_i + x_i \cdot d_i \cdot 2^{-i+1} \\ z_{i+1} &= z_i - d_i \cdot \tan^{-1}(2^{-i}) \end{cases} \quad (3.44)$$

$$d_i = -1 \text{ if } z_i < 0, \quad +1 \text{ otherwise}$$

It requires 4-shift and 5-add operations per iteration stage, as shown in Fig.3.8. The results after a finite number of iterations is

$$\begin{aligned} x_n &= A_n^{(ii)} (x_0 \cos z_0 - y_0 \sin z_0) \\ y_n &= A_n^{(ii)} (y_0 \cos z_0 + x_0 \sin z_0) \\ z_n &= 0 \\ A_n^{(ii)} &= \{A_n\}^2 = \prod_{i=0}^n (1 + 2^{-2i}) \end{aligned} \quad (3.45)$$

In Eq.(3.45), the computational gain $A_n^{(ii)}$ becomes square root operation free. In addition, double rotation makes the division operation free in the scaling factor as Eq.(3.46). This is because for a given precision b of the shift and add operations, all factors $(1 - 2^{-n})$ with $n > b$ do not contribute to $K_n^{(ii)}$. Thus, the scaling factor can be approximated to a simplified form as

$$\begin{aligned} K_n^{(ii)} &= \{K_n\}^2 = \prod_{i=0}^n \frac{1}{1 + 2^{-2i}} = \frac{1}{2} \prod_{i=1}^n \frac{1 - 2^{-2i}}{1 - 2^{-4i}} \\ &\approx \frac{1}{2} \prod_{i=1}^{n/4} (1 - 2^{-(4i-2)}), \end{aligned} \quad (3.46)$$

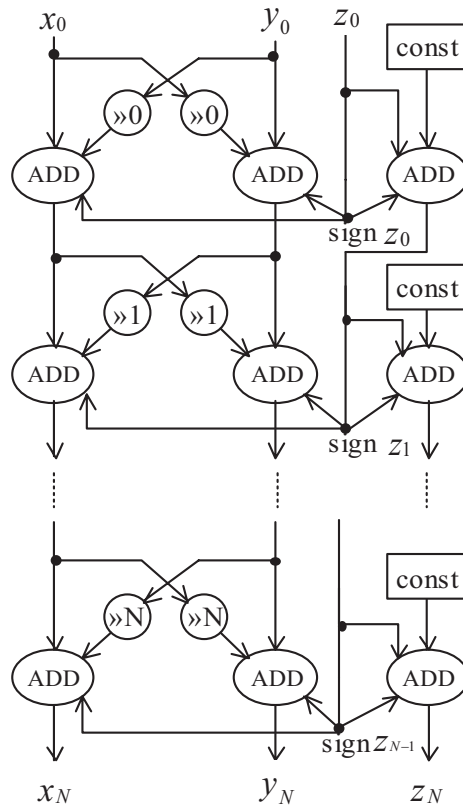


Fig. 3.7: Unrolled CORDIC Architectures (Rotation Mode)

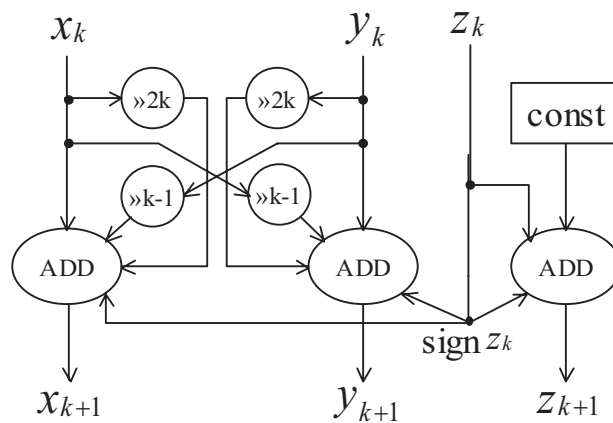


Fig. 3.8: k -th stage of double rotation (Rotation Mode)

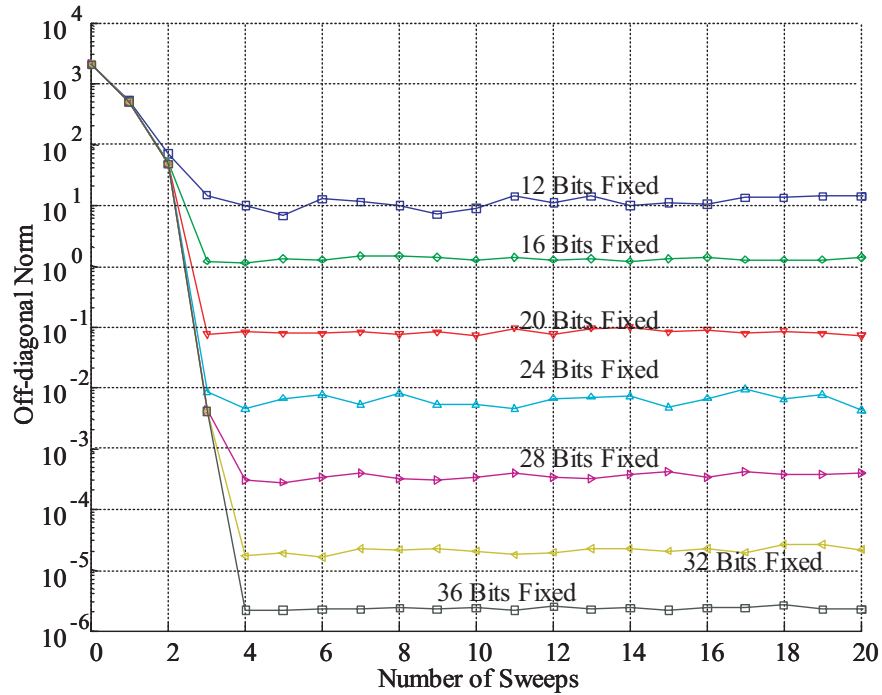


Fig. 3.9: Reduction of off-diagonal norm with various word-length (6×6 random real symmetric matrix).

which can also be computed only with shift and add operations [98]. Fig.3.8 shows the k -th stage of the double rotation. In this work, double rotation unrolled architecture is used for efficient fixed-point implementation.

3.4.3 Fixed-Point Implementation

This section describes the fixed-point implementation of Jacobi EVD processor based on CORDIC. The required number of Jacobi sweeps, the appropriate precision (word-length) for the desired accuracy, and the applicability to the MUSIC DOA estimator are examined. First, it is necessary to determine the number of Jacobi sweeps required to provide the desired convergence level.

Figure 3.9 illustrates the reduction of off-diagonal norm to the number of Jacobi sweeps with a 6×6 random real symmetric matrix of, for example, 12-bit precision. The off-diagonal reduction is defined as Eq.(3.34) and the lower value implies that it is closer to the diagonal matrix. On general-purpose computers, the 32-bit floating-point operation by the C language converges to the machine zero within a given precision after several Jacobi sweeps; however, Fig.3.9 shows that fixed-point arithmetic does not converge but keeps vibrating from 12 to 36 bits after approximately four Jacobi sweeps regardless of the precision. This is caused by the limited precision of the fixed-point operation. At the cost of computation accuracy, the fixed-point operation achieves simpler circuit implementation, high performance, and low power consumption. Without using an additional convergence decision circuit, fixing the

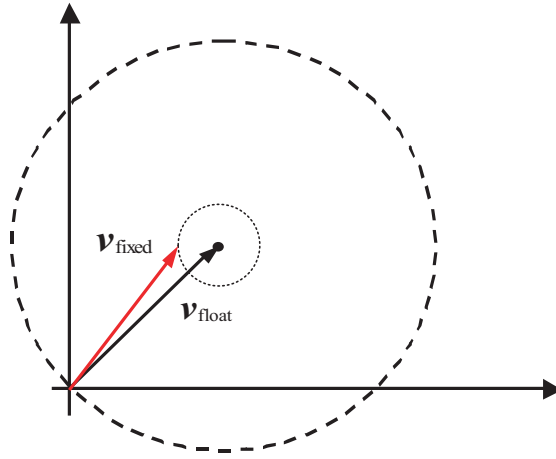


Fig. 3.10: Errors between vectors.

number of sweeps at four may be an appropriate choice. Further, greater accuracy cannot be achieved even with the execution of more Jacobi sweeps. Since a finite number of operations are determined in advance, it can always be computed in the same computation time.

Next, the precision of fixed-point arithmetic should be examined. Accuracy within an allowable error range should be guaranteed in order to verify a fixed-point system operation. Eq.(3.47) yields the error ratio where \mathbf{v} 's are the vectors whose elements consist of eigenvalues computed in the subscripted ways. Further, $\|\cdot\|$ denotes the vector norm, and the error between vectors is defined by

$$\text{Error} = \frac{\|\mathbf{v}_{\text{float}} - \mathbf{v}_{\text{fixed}}\|}{\|\mathbf{v}_{\text{float}}\|} \quad (3.47)$$

as shown in Fig.3.10.

Fig.3.11 shows the error ratio of the fixed-point arithmetic with various bit-lengths on the CORDIC-Jacobi EVD processor with respect to the 32-bit floating-point operation on general-purpose computers⁴. Fig.3.11 uses a 6×6 random real symmetric matrix of 12-bit precision as an input matrix. The longer the word-length in the fixed-point arithmetic, the greater is the accuracy that can be achieved. When it was implemented with more than 16-bit precision, it had less than 0.5% error in the floating-point operation. Approximately 16-bit precision is desirable for practical use. In this paper, the computational load of the processor and the word-length are four Jacobi sweeps and 16-bit, respectively.

Regarding the application of the fixed-point arithmetic, the computation accuracy in a practical application should be carefully examined. The fixed-point effect on the computation accuracy was quantitatively calculated. For example, Fig.3.12 shows the result of the DOA estimation performed by the spectral MUSIC method assuming that two waves arrive at the 4-element linear array antenna. The simulation results are sufficiently good for the peaks to appear at precisely the same angles as the floating-point spectrum, where the EVD was

⁴It implies that The 32-bit floating-point operation with float type (single precision) in a C compiler with an Intel Pentium machine.

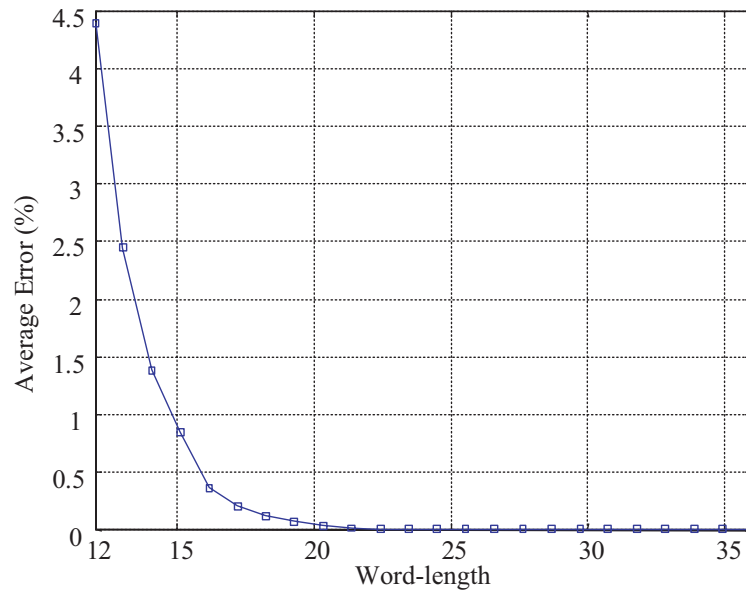


Fig. 3.11: Average error ratio of fixed-point operations to 32-bit floating point operation (6×6 random symmetric matrix).

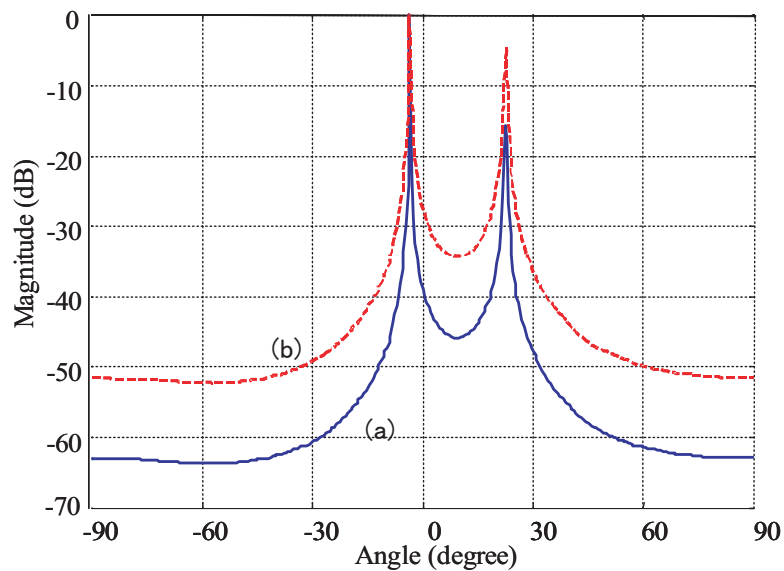


Fig. 3.12: MUSIC Spectrum in case of 4-element array antenna and two incident waves (DOAs are -5° and 20° with $\text{SNR} = 20\text{dB}$); (a) 32-bit floating-point operation with a general computer and (b) 16-bit fixed-point operation by the CORDIC-Jacobi EVD processor

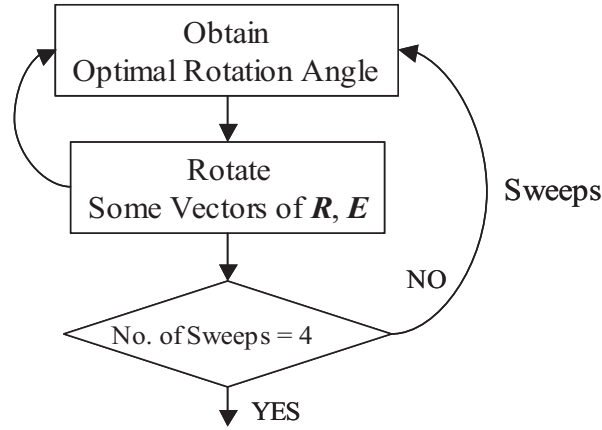


Fig. 3.13: Computation Flow of Cyclic Jacobi EVD Processor

computed by 32-bit floating-point arithmetic on a general-purpose computer and 16-bit fixed-point arithmetic on a proposed Jacobi EVD processor based on CORDIC. In this simulation, except for EVD computation all the other processes of the MUSIC method, such as correlation matrix, spatial smoothing, and MUSIC spectrum were computed on the general-purpose computer with a floating-point operation.

3.4.4 Processor Structure

As mentioned above, approximately four Jacobi sweeps are sufficient for convergence, and the fixed-point operation with a 16-bit word-length gives a good spectral estimation result. Based on these facts, this section proposes FPGA implementation of the EVD processor.

Fig.3.13 shows the computational flow of Cyclic Jacobi EVD processor. As described earlier, the Jacobi type EVD is a very simple algorithm and is merely an iterative process of vector rotations until the desirable convergence level is achieved. The optimal rotation angle is determined from Eq.(3.37) and subsequently, the processor performs a similar transformation of correlation matrix \mathbf{R} and unitary matrix \mathbf{E} (initial value is identity matrix \mathbf{I}) of eigenvectors. After four Jacobi sweeps, the computation is complete, the resulting matrix \mathbf{R} converges to the diagonal matrix of eigenvalues, and \mathbf{E} becomes the unitary matrix of the eigenvectors with the given precision.

The EVD processor consists of CORDIC vector rotators and CORDIC arctangent computers. With an optimum angle obtained by Eq.(3.37), the rotation \mathbf{W}_{pq} is determined as Eq.(3.31). The transformation \mathbf{W}_{pq} in Eq.(3.32) changes only the p -th and q -th rows and columns of the matrix \mathbf{R} . Therefore, the transformation can be simplified as

$$\begin{pmatrix} \mathbf{r}'_p \\ \mathbf{r}'_q \end{pmatrix} = \mathbf{w}_{pq}^T \cdot \begin{pmatrix} \mathbf{r}_p \\ \mathbf{r}_q \end{pmatrix} = \begin{pmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{pmatrix} \cdot \begin{pmatrix} r_{p1} & \cdots & r_{pp} & \cdots & r_{pq} & \cdots & r_{pN} \\ r_{q1} & \cdots & r_{qp} & \cdots & r_{qq} & \cdots & r_{qN} \end{pmatrix}, \quad (3.48)$$

where \mathbf{r}_k and \mathbf{w}_{pq} denote the k -th row vector of the matrix \mathbf{R} and the (p, q) plane rotation that

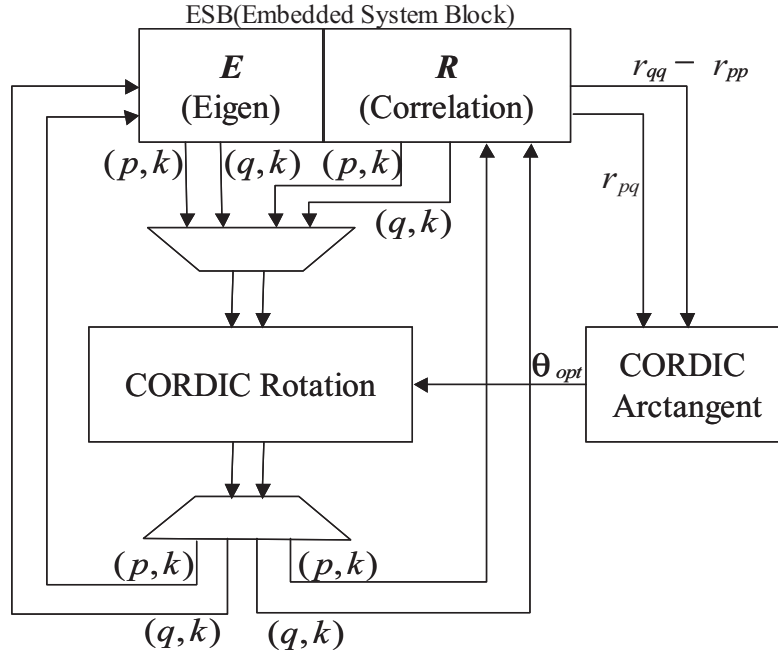


Fig. 3.14: Architecture of EVD processor core.

is a sub-matrix of \mathbf{W}_{pq} in Eq.(3.31), respectively. The right side transformation in Eq.(3.32) yields the same result due to the symmetric property of the matrix \mathbf{R} ; hence, it does not need to be considered if the second rotations of only two vectors $[r_{pp} \ r_{qq}]^T$ and $[r_{pq} \ r_{qq}]^T$ are performed again.

The most interesting feature between the QR and Jacobi methods to the symmetric eigenvalue problem is the rith inherent parallelism of the latter one. By grouping non-conflicting rotation, parallel rotation can be performed [96]. That is, $N(N-1)/2$ rotations for a Jacobi sweep are grouped by $(N-1)$ sets consisting of $N/2$ non-conflicting rotations; hence, the complexity can be decreased by $O(N^2)$ from $O(N^3)$. In the CORDIC matrix rotator, the CORDIC vector rotators are simultaneously performed with multiple processors using the inherent parallelism of dedicated circuit. It takes $N(N-1)/2$ matrix rotations per sweep to compute \mathbf{R} and \mathbf{E} . Fig.3.14 illustrates the architecture of the EVD processor core, where the ESB (Embedded System Block) is a memory block of an FPGA and stores the correlation matrix and eigenvector matrices.

3.4.5 Computational Load and Expected Performance

The basic arithmetic operation of the EVD processor consists of only shifts and adds. In the double rotation CORDIC stages, the computational load yields

$$\left(4B + \frac{1}{4}B\right) \text{ Shifts and } \left(5B + \frac{1}{4}B\right) \text{ Adds,} \quad (3.49)$$

where B is the word-length and $1/4B$ is approximately taken for scaling operation from Fig.3.8 and Eq.(3.46). The number of vector rotations required for computing both eigenvalues and

eigenvectors is $4N(N-1)(N+2)$. This is because \mathbf{E} performs 4 \mathbf{J} 's, \mathbf{J} consists of $N(N-1)/2$ \mathbf{W} 's, and \mathbf{W} requires $(N+2)$ vector rotations from Eq.(3.30), where N is the matrix dimension⁵. Therefore, by addition of the arctangent, the total computational load of the CORDIC-Jacobi EVD processor is

$$[4N(N-1)(N+2) + 1] \times \left(\frac{17}{4}B \text{ Shifts} + \frac{21}{4}B \text{ Adds} \right). \quad (3.50)$$

On the other hand, a rough estimate of the circuit scale obtained by configuring this computational load with the parallel architecture is approximately $(N+1) \times 15K$ equivalent gates (single 16 bit-CORDIC processor could be synthesized using approximately $15K$ equivalent gates). For example, if $N = 8$ (4-element array antenna with real matrix extension and no spatial smoothing) the total circuit scale is approximately $75K$ equivalent gates. The estimated result is obtained by synthesizing the circuit described by VHDL (Very high speed integrated circuit Hardware Description Language) with the Leonardo Spectrum, Exemplar Logic Inc., where the target device was Altera's FPGA, APEX20KC [102].

If this computation load is configured by the parallel circuit architecture and one clock cycle is required for the shift or add operation (worst case scenario), the first EVD result appears after

$$[4 \times N(N-1) \times 2 + 1] \times (B+1) \quad (3.51)$$

clock cycles. For example, if $N = 6$, $B = 16$ (in the case of 4-element array antenna and spatial smoothing with 2 sub-arrays of 3 sub-elements), and the operation is performed at the speed of 100 MHz, this system can compute EVD computations at approximately 13,200 times/sec ($75.8 \mu\text{s}/\text{EVD}$). It is noteworthy that the pipeline processing performed by appropriately placing the register can achieve higher performance than that shown by the above example.

Taking into consideration the high-speed mobility under higher frequencies in next-generation communication, it is very difficult to realize the required performance for the robust system to fast fading with general-purpose processor. This proposed EVD processor is basically made of a combinatorial logic circuit. At present, advances in circuit technology are thought to offer high-speed operation of a general combinatorial logic circuit. Such a fast EVD processor can be of practical use in various applications.

⁵In array antenna processing where the array length is N , N -by- N correlation matrix with complex numbers can be computed by conversion into an extended form of $2N$ -by- $2N$ matrix of only real numbers [97]. It is possible to apply the unitary transformation for the real number correlation matrix without extension of the matrix dimension.

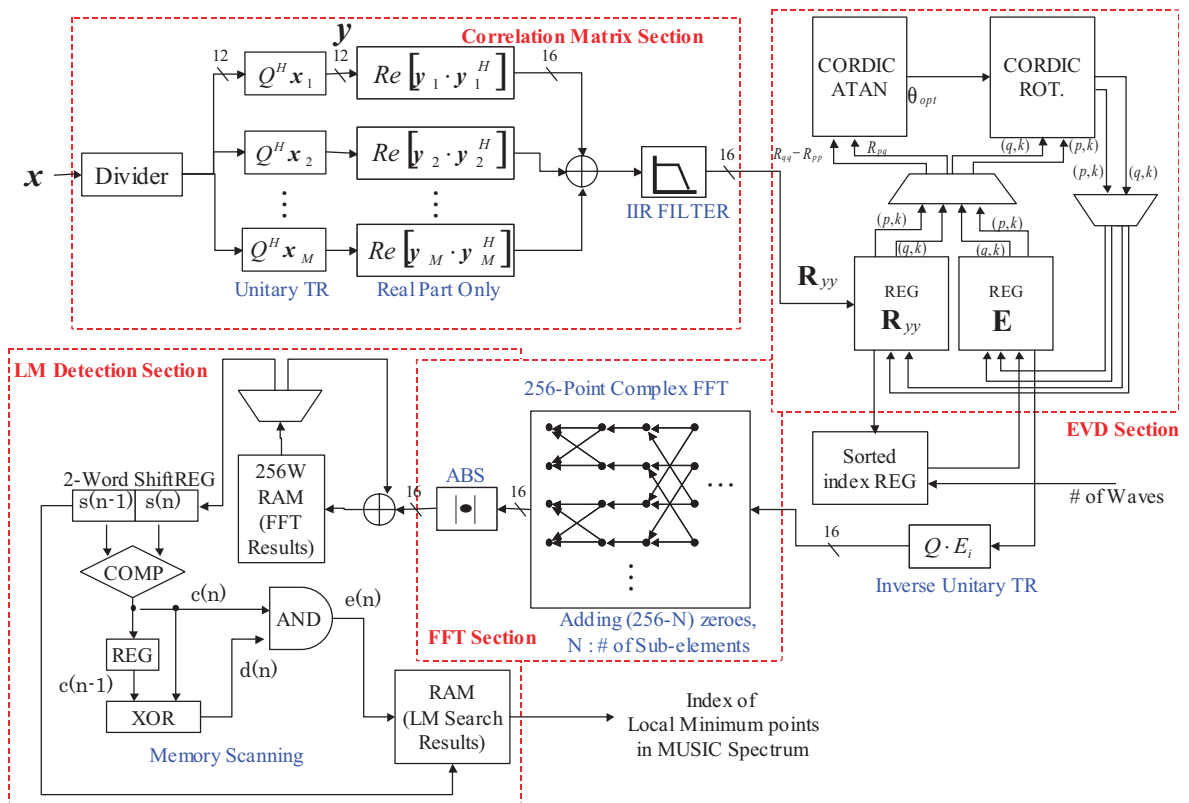


Fig. 3.15: Block diagram of UMP digital signal processor.

Table 3.1: Core performances of dominant procedures (4-element with SS).

	Required Clocks (M_{clk})	LEs (Logic Elements)	f_{max} (MHz)	t_{min} (μs)
$\hat{\mathbf{R}}_{yy}$	N	8,301	27.4	$0.04 \times N$
EVD	1,836	4,045	110	16.69
FFT & LM Detection	1,356	2,303	114	11.89

3.5 Hardware Implementation

The actual implementation was also attempted on single FPGA⁶. The entire block diagram of the digital signal processing procedures is shown in Fig.3.15. This is involved in 4 major procedure sections-Correlation Matrix Section, EVD Section, FFT Section, and LM Detection Section. The word-length of every section is shown in this figure. It is assumed that the exact number of waves were predetermined and already known from any other pre-processing method. The procedures with VHDL (Very high speed integrated circuits Hardware Description Language) have also been described⁷.

Table 3.1 illustrates the roughly estimated performance of the dominant processing cores, where LEs (Logic Elements, see Fig.2.4) represents the number of occupied logic blocks in FPGAs and f_{max} is the maximum clock frequency at which normal operation can be guaranteed. The minimum computation time t_{min} is calculated by $M_{\text{clk}}/f_{\text{max}}$, and N is the number of snapshots. In this chapter, in order to reduce system complexity, we assumed a 4-element uniform linear array (ULA) antenna and that the number of coherent/incoherent waves arriving at the antenna is two. A 256-point radix-4 complex FFT was employed to generate spatial frequency spectrum [104], the FFT with 256 spatial samples composed of 3 elements of the noise eigenvector (1 dimension of array freedom is used for spatial smoothing), and $(256 - 3)$ zeroes are interpolated to ensure that the spectrum is fine and smooth. All the computations were performed by fixed-point arithmetic with 12-bit input data from ADCs. As shown in Tab.3.1, if FFT was performed only once in a 4-element UMP with spatial smoothing (in the presence of two incident waves), EVD had the largest computational load. The pipeline scheduling enables us to divide the entire processing into sub-blocks. That is, if the three sub-blocks illustrated in Tab3.1 are considered, this system can perform single realization of DOA estimation within approximately $17 \mu\text{s}$. The inherent parallelism and optimizability of FPGAs resulted in the fast computation performance. In addition, the recent FPGA manufacturing technology allowed for low electric power consumption at less than approximately 2 watts.

Figures 3.16 and 3.17 show the entire evaluation system configuration and its appearance,

⁶The implementation was attempted using three different FPGAs-APEX20KC, STRATIX EP1S25, and STRATIX EP1S40 by Altera. For example, STRATIX EP1S25 has approximately 0.6 million equivalent gates, 200 Kb internal memory blocks, and optimized digital signal processing (DSP) blocks [103].

⁷The VHDL sources were synthesized and place-and-routed by Leonardo spectrum (Exemplar Logic Inc.) and Quartus II (Altera).

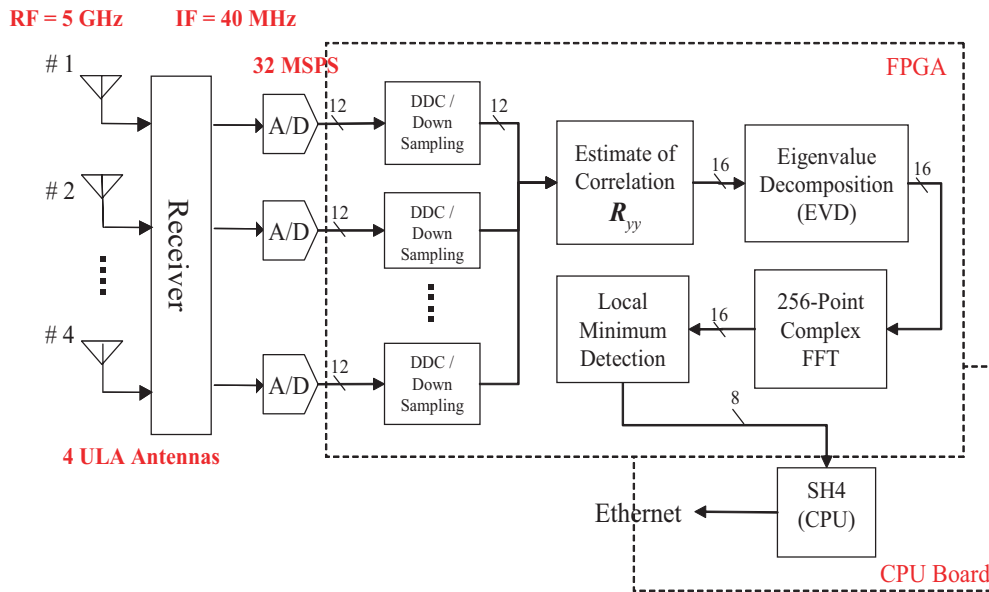


Fig. 3.16: Hardware configuration of DOA estimator.

respectively. The system architecture is a super-heterodyne IF sampling receiver with quasi-coherent detection as mentioned in Chapter 2. RF signals received at an antenna array are downconverted to IF band in analog downconversion receiver, where the RF and IF frequencies are 5 GHz and 40 MHz, respectively. The IF signals are then digitized by ADCs at the rate of 32 MSPS. The undersampled IF signals are again digitally downconverted to complex baseband and subsequently downsampled L -times, where L is an appropriate integer number. As shown in Fig.3.16, single FPGA on AD board performs the digital signal processing of UMP. The user terminal PC communicates with the CPU SH4 via Ethernet, and the CPU controls the UMP via direct 32-bit data bus connection.

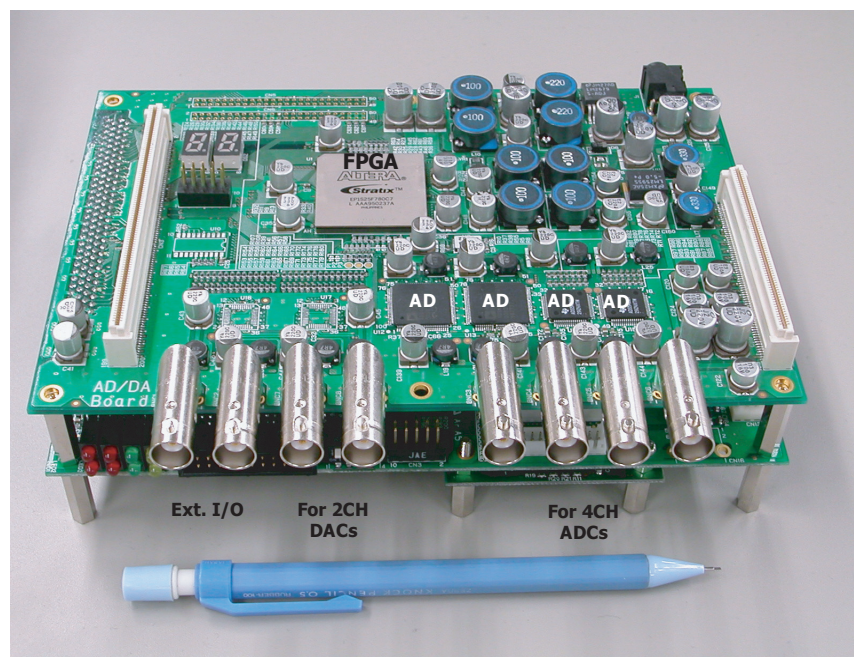


Fig. 3.17: Appearance of UMP digital processing unit integrated on 4-channel prototype board.

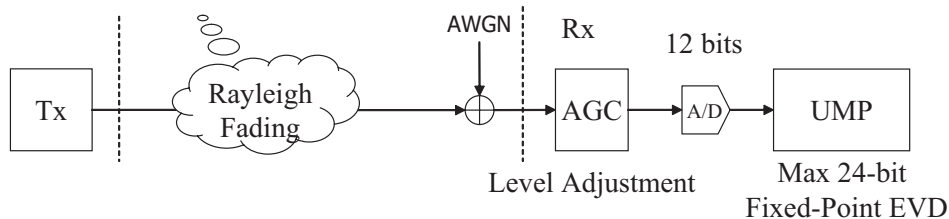


Fig. 3.18: Equivalent baseband simulation model.

3.6 Performance Assessments

The performance of MUSIC DOA estimation technique has been studied theoretically [34, 37–39]. However, in this section, the performance in the designed fixed point system is examined. We discuss the estimation performance of the UMP by hardware simulations with Matlab (Math works) on an offline PC. Hardware simulations imply that the fixed-point operation behavior of UMP in VHDL was perfectly described in Matlab m-file. It was assumed that the antennas and analog components prior to UMP had ideal characteristics or those that were well calibrated. In other words, these simulations considered the digital signal processing part only and neglected all system-specific effects of analog parts. It would be more efficient to assess the system without operating the entire system components for various cases. An input level adjustment circuit, such as AGC (Automatic Gain Control), was considered in order to utilize the full scale range of ADCs (typically 12 bits); the performance of UMP would otherwise be degraded because of the low dynamic range of the fixed-point operation with bit truncation. The equivalent baseband simulation model is illustrated in Fig. 3.18. In this section, all the simulations included 200 burst frame data where a single burst consisted of 136 snapshots (symbols). The source waves were $\pi/4$ -shift QPSK modulated signals.

3.6.1 Noise Channel under Planar Wave Assumption

In the AWGN channel, the standard deviation of the estimated DOA is a good overall performance assessment of an estimation variation to input SNR when the single wave is impinging from broadside. A similar approach has been used in [66]. Figure 3.19 shows the simulation results computed by the 4-element UMP using 16-bit fixed-point operation with spatial smoothing (SS) and by the offline PC with 64-bit floating-point (double precision) operation⁸, where the diamond, right-triangled, and left-triangled lines denote the incident DOAs of 0, 30, and 50 degrees, respectively. In addition, the results of 4- and 8-element UMP without SS at 0 degrees are also illustrated by the squared and circled lines, respectively.

Based on these results, it is clear that the estimation variation is below 2 degrees if the input SNR is greater than 5 dB within the linear region between -30 and +30 degrees. Further, it can be quantitatively confirmed that the estimation variation could be improved by the use of more antennas. The UMP performs well for an offline PC, although the estimation variation

⁸In Matlab, all numbers are stored internally using the long format (64-bit double precision) specified by the IEEE floating-point standard.

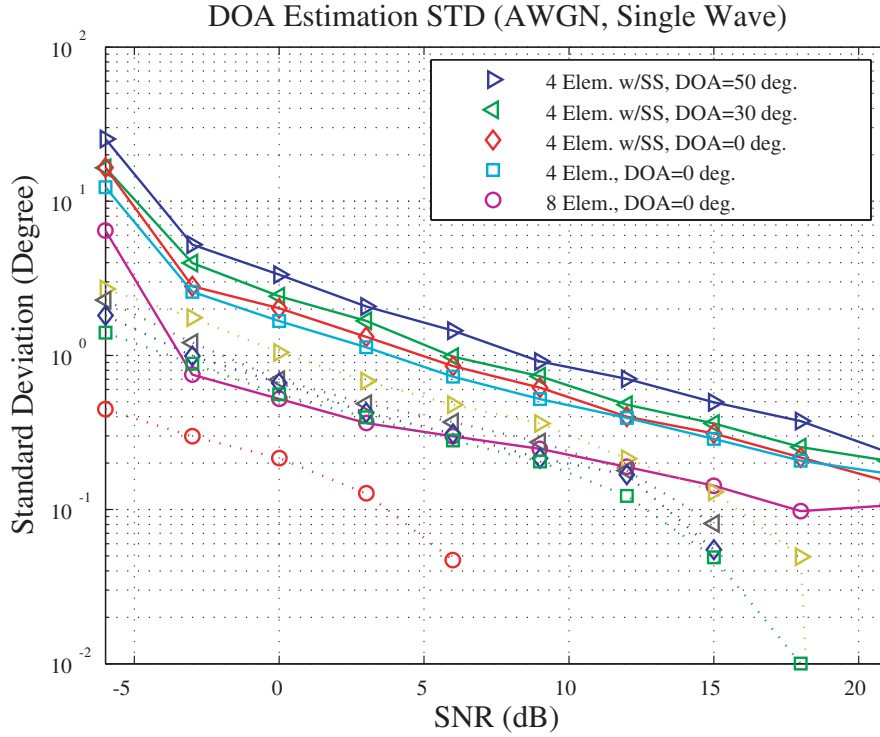


Fig. 3.19: Standard deviation of estimated DOA when single wave impinging at 0, 30 and 50 degrees from broadside.

is larger by some degrees because of its finite word-length (16-bit) fixed-point operation. In fact, it can be observed that the floating-point operation has SNR gain that is approximately 10 dB more than the fixed-point operation; this, however, is an unavoidable trade-off between the two. In Fig.3.19, the estimation variation increases as the DOA moves away from the broadside. If an ideal omni-directional antenna pattern is considered, this will be caused only by the non-uniform discrete wavefronts generated by the spatial DFT. The non-uniform discrete wavefront effect is illustrated in Fig.3.20, which shows the DOA dependency of the mean DOA deviation ϑ , where

$$\vartheta = E\{|\theta_{\text{estimated}} - \theta_{\text{true}}|\}. \quad (3.52)$$

In the case of multiple incident waves, the separability performance representing the manner in which two waves, which are spatially close, can be distinguished from each other can be applied when there exist multiple incident waves. The problems are simplified by considering only two incident waves. The criteria of the successful estimation was

$$r^\varphi = \arg \max_{\theta} \{\mathcal{R}_{\text{std} < \rho}^\varphi \cap \mathcal{R}_{\text{mean} < \rho}^\varphi\}, \quad (3.53)$$

where φ , θ , and ρ are the given SNR, the incident DOA, and the condition value, respectively. r^φ and \mathcal{R}^φ denote the separable angle and the range of θ satisfying subscripted condition to each estimation at the given SNR φ , respectively. In this case, the condition of (mean $< \rho$)

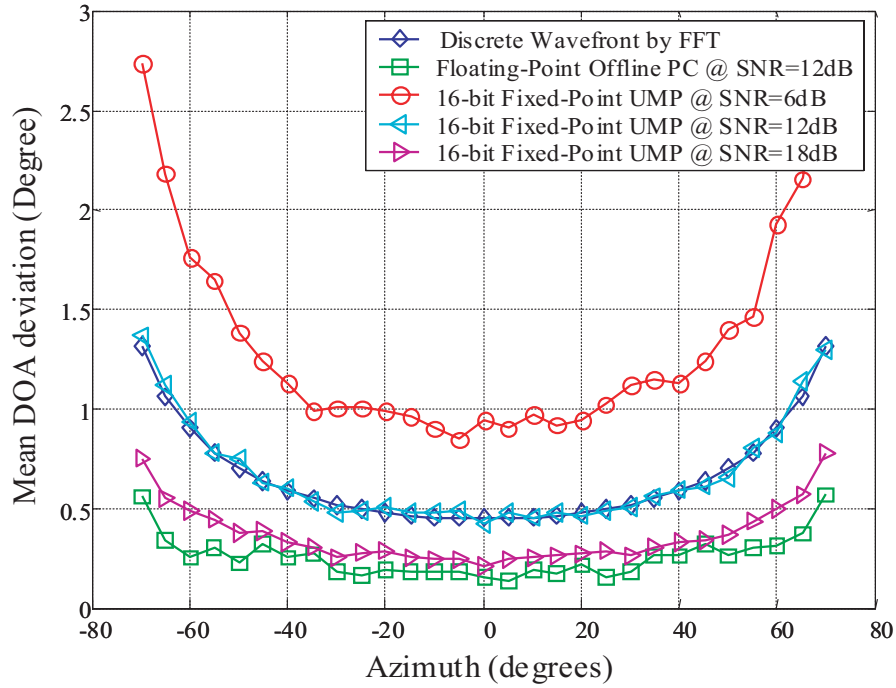
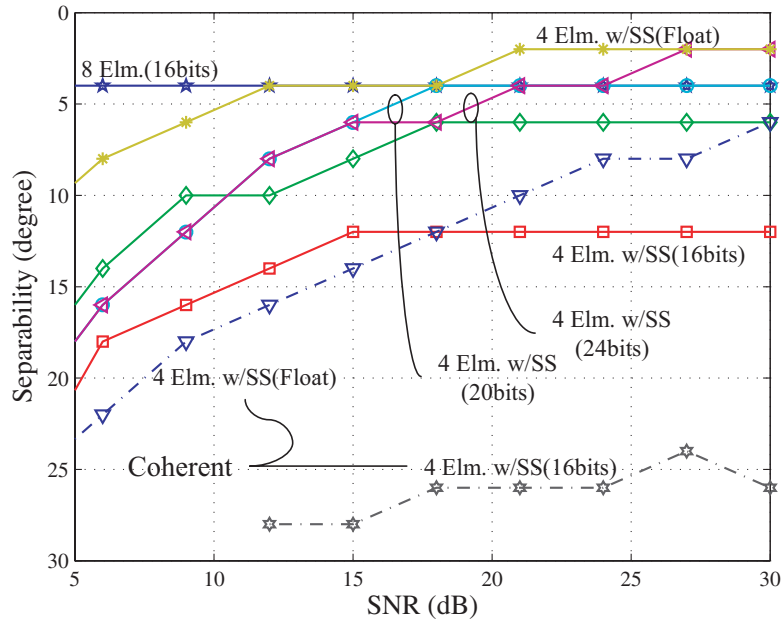
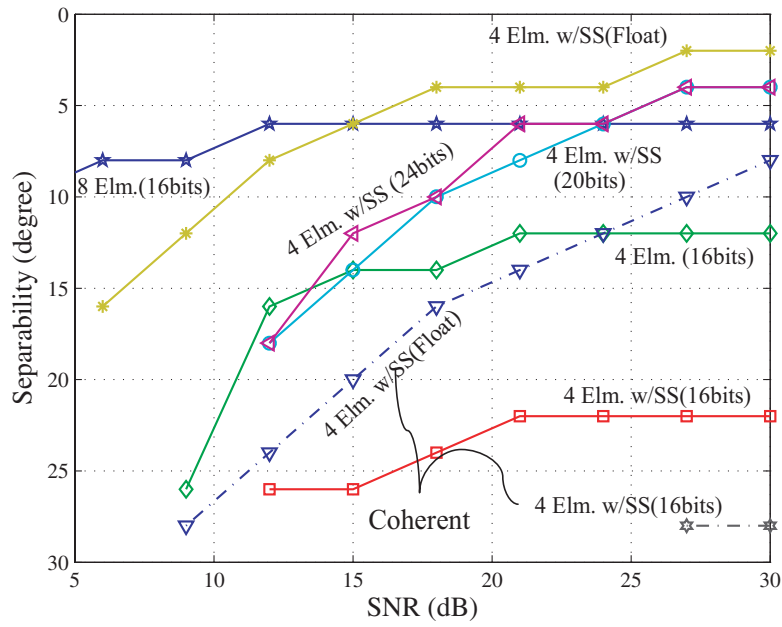


Fig. 3.20: DOA dependency of estimation performance.

eliminates far-off estimation with small variations in the estimation. Figure 3.21 shows the separability performance of the UMP where the solid and dotted lines denote incoherent and coherent waves, respectively. The two waves had identical powers. The spatial smoothing (SS) capability to reduce the correlation of two coherent waves by a few degrees. In Fig.3.21, the separability performance of the UMP increases as the EVD word-length gets longer; however, it is degraded if the two waves are highly correlated (coherent). This occurs because the SS with two sub-matrices in fixed-point arithmetic cannot provide sufficient reduction of the correlation between two waves. However, this will be improved with larger number of sub-matrices in a longer array antenna and longer word-length computation. The 16-bit fixed-point 4-element UMP without SS can separate two close incoherent waves, the DOA difference of which is approximately 10 degrees when the SNR is greater than 10 dB under the condition of $\rho = 3^\circ$, as shown in Fig.3.21 (a).



(a) $\rho=3$ deg.



(b) $\rho=1$ deg.

Fig. 3.21: Separability performance of two incident waves.

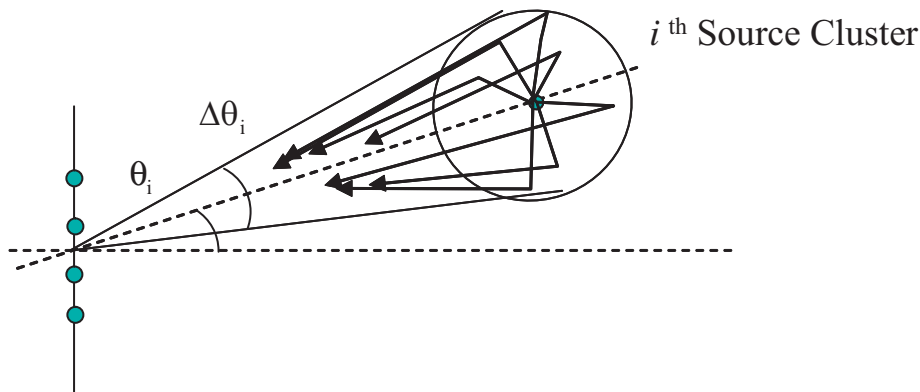


Fig. 3.22: Angle spread model.

3.6.2 Multipath Channel with Small Angle Spread

The above analysis would be fairly important in evaluating the behavior of the fixed-point UMP at a given SNR. However, the practical channel was not appropriately modeled in the above simulations. In wireless cellular communication, the fading phenomenon occurs by multipath propagation. In such a fading environment, the SNR becomes a random variable with any distribution. In addition, the large number of coherent signals caused by far field local scatterers arrives from spread DOA to reduce the fading correlation between antenna elements. Based on this, the plane wave model from point sources may not be valid. Thus, the estimation performance is usually degraded in a multi-path fading environment [40]. Considering this, it is extremely important to investigate the behavior of UMP assuming a multi-path fading environment. Cellular base station applications were considered in this study. The signals at the base station are received through the scattering process in the local scatterers around the mobile station because the antenna is usually deployed higher than the surrounding scatterers, as shown in Fig.3.22. In this case, the fading across the antenna elements spaced by $\lambda/2$ is still highly correlated and the AS is typically only a few degrees. In such an AS model, the time delays among the sub-paths can be neglected. Hence, the channel vector for the i -th source in Eq.(3.2) can be rewritten approximately as

$$\mathbf{v}_i = \sum_{j=1}^{N_i} \beta_{ij} \mathbf{a}(\theta_i + \tilde{\theta}_{ij}), \quad (3.54)$$

where

β_{ij} : Complex amplitude with Rayleigh distributed magnitude of j -th scattered sub-path

$\tilde{\theta}_{ij}$: DOA deviation of Gaussian random variable $\sim \mathcal{N}(0, \sigma_{\tilde{\theta}_i}^2)$

N_i : Number of sub-paths for i -th source

and $2\sigma_{\tilde{\theta}_i}$ is defined as AS. The relationship between the AS and estimated mean DOA deviation, as given by Eq.(3.52), is shown in Fig.3.23, where $N_1 = 30$ sub-paths are uniformly distributed at the center of single wave source located at $\theta_1 = 30^\circ$ and average SNR is 10 dB. In this

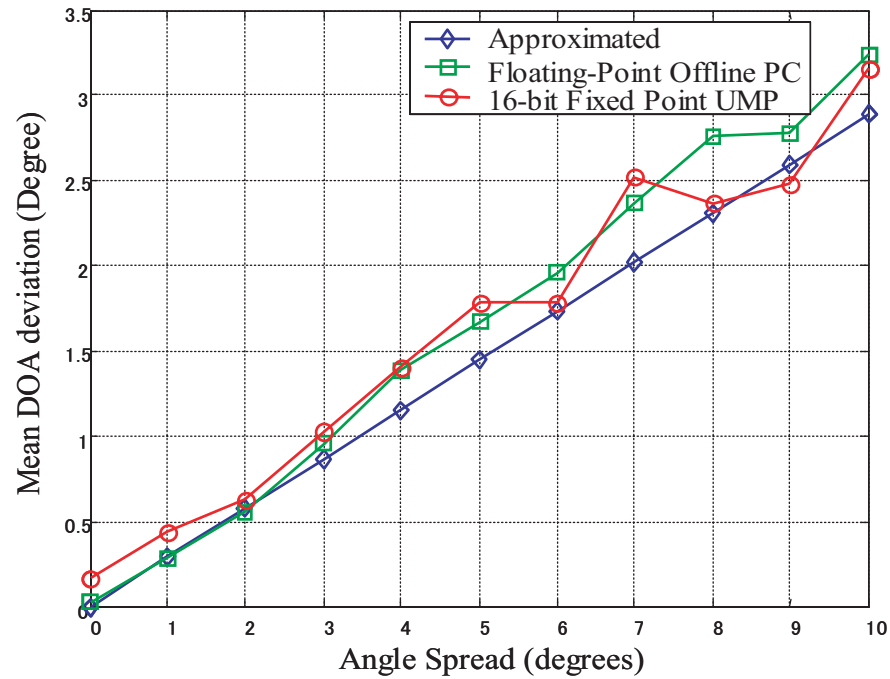


Fig. 3.23: Mean DOA deviation to angle spread in UMP (average SNR=10dB).

figure, the diamond line is the theoretically approximated result [40]. The UMP result is in good agreement with the theoretical approximation. Hence, the functionality of UMP in a realistic multipath channel model is observed to be still valid.

Table 3.2: Experimental parameters.

Antennas	4-element sleeve antenna in ULA
Antenna spacing	$\lambda/2$
RF frequency	5 GHz
IF frequency	40 MHz
Modulation	CW
Sampling frequency	32 MHz
ADC resolution	12 bits

3.7 Real Data Examples

In this section, the entire system operation of the UMP will be experimentally demonstrated in a radio anechoic chamber. A 4-element omni-directional sleeve antenna array that was half wavelength equi-spaced in linear geometry was used. The fine-calibration procedure was not performed in this experiment; however, the coarse adjustment of amplitude and phase was manually conducted before measurement⁹. This example assumed two incident waves, and the data snapshot vector of these waves was generated by a linear combination of each data snapshot vector of the single incident wave. The experimental parameters are illustrated in Table 3.2. The RF carrier frequency was 5 GHz. The transmitted waves were CW at different frequencies (the difference was approximately 1.3 MHz). Figure 3.24 shows the experimental result. The DOAs of each wave were set by 0 and 40 degrees. Two waves were transmitted at the same power, and the average SNR at each antenna element was approximately 19 dB. In Fig.3.24, the indices of the DFT spectrum corresponding to the LM points below any appropriate threshold level (relative fixed point level of 5,000 herein) were 127 and 208. With these indices, the concrete discrete wavefronts could be converted to -0.4476 and 38.6822 degrees from the relationship given by Eq.(3.27), respectively. The additional estimation error was caused by the lack of the fine calibration for the antennas and analog components; however, the system operation could be sufficiently confirmed. In reality, the calibration of the entire system should be cleared for practical use.

⁹Fine calibration implies the compensation of the mutual coupling effect among branches of antennas and receivers. The array calibration will be discussed in Chapter 5.

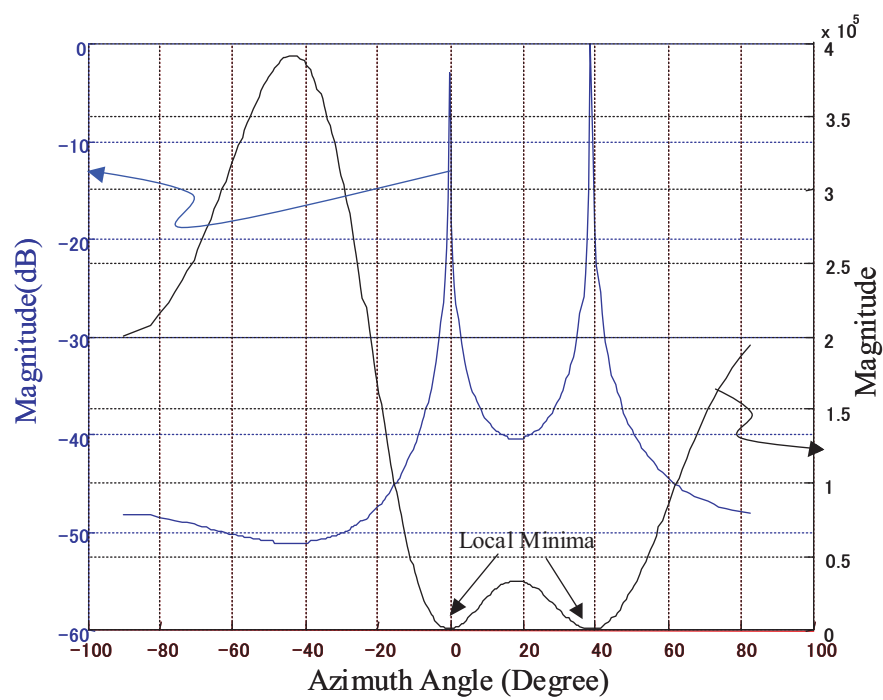


Fig. 3.24: Experimental result of MUSIC spectrum and its reciprocal (4 antennas, two waves impinging at 0 and 40 degrees, same powers, average SNR=19 dB).

3.8 Summary

In this chapter, the FPGA design of the fast DOA estimator using the unitary MUSIC algorithm was proposed, and its real hardware implementation was also introduced. The unique features of this system are fast computation and compact architecture of the EVD and MUSIC angular spectrum generation with the Cyclic Jacobi processor based on CORDIC and spatial DFT, respectively. All procedures of digital signal processing were computed by fixed-point operation with only finite word-length for high speed and low power consumption. Regarding the optimization, which depends on the design technique, the hardware friendly parallel algorithm and processing concept will be still valid and outperform the serial architected computer like general-purpose CPU.

Chapter 4

DOA-based Beamforming Processor

4.1 Introduction

A smart antenna beamforming system based on the DOAs of incident signals as the spatial channel information has certain significant advantages over the temporal reference-based techniques of combining techniques in specific environments. The first advantage is that the DOA-based beamforming has superior SINR performance compared to that of other techniques of combinations for small AS [16]. This might be reasonable in macro cellular suburban environments having local scatterers around a mobile terminal. In addition, they are directly applicable to the downlink (forward link) beamforming because of the knowledge of explicit directional information; hence, the base stations can steer maximum transmitting power toward the desired user direction. However, the drawback is that the DOA estimation is a time-consuming task. Furthermore, almost all DOA based beamforming techniques usually require complex and large computation loads, such as inversion of the complex valued correlation matrix for the SIR or SINR optimization problems. In reality, the performance depends on the DOA estimation accuracy and channel condition, such as AS. On the other hand, a low-sidelobe beamformer, such as the DC-BF, is an alternative approach as a result of its low complexity. The DC-BF only requires the DOA of the user signal steering its direction with a quiescent beam. Further, the interferers are totally suppressed by an equi-rippled low sidelobe.

This paper introduces a simple and safe beamforming technique with a low-sidelobe beam-pattern using the Dolph-Chebyshev (DC) tapering window. It has extremely low complexity with a simple amplitude weighting operation that is also suitable for implementation on high-speed logic devices such as FPGAs. High-speed weight adaptation capability due to its low complexity may be extremely useful for applications in various wireless communication systems for fast fading environments. In addition, equi-ripple low sidelobe leads to reasonable interference suppression performance in an AS environment. However, broadened beamwidth caused by low-sidelobe beam-pattern affects the angular resolution; hence, the SINR performance will be degraded if the source separation between the signal of interest and the adjacent interferer is small for its beamwidth. The relationship between low sidelobe and beamwidth is an inherent trade-off. In this study, a novel approach with cascade beamforming architecture will be proposed resolving the drawback of beamforming with low-sidelobe beam-pattern.

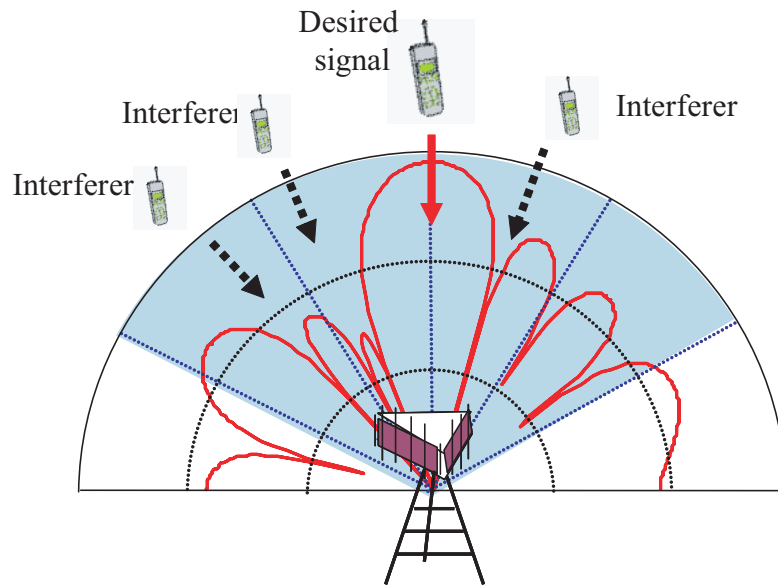


Fig. 4.1: Adaptive beamforming operation in cellular basestation (uplink).

This chapter, at first, surveys DOA-based beamforming systems using estimated DOAs of the incident signals and proposes a novel beamforming technique, as mentioned above. Hardware implementation using an FPGA will be also introduced.

4.2 DOA-based Beamforming Techniques

Digital beamforming can improve the SINR performance by adaptively controlling the directivity of the antenna radiation pattern, as shown in Fig.4.1. Several excellent optimum beamforming algorithms, such as Minimizing Mean Square Error (MMSE), Directional Constrained Minimizing Power (DCMP), and Maximum SNR (MSN) techniques [4, 5, 7, 12], have been studied already. In addition, zero-forcing (ZF) technique based on channel response estimation can be considered as another choice; it forces zeros in interferers' directions on the antenna pattern [1, 53].

This paper assumes that the DOAs of incident signals are estimated and that their user signal is identified in advance by the DOA estimation process. Further, beamforming is performed based on the estimated DOA information. There exist optimum beamformers, such as DCMP and ZF with null-steering function, and low-sidelobe DC-BF with beamforming for the desired signal, as illustrated in Fig.4.2.

4.2.1 Optimum Beamformers

DOA-based optimum beamforming techniques include DCMP and ZF. However, these techniques require solving the (pseudo) inversion of the correlation matrix from the generalized eigenvalue problem that has high complexity. In the ZF technique, the sharp nulls will decrease the interferer rejection performance in AS environments as well as well-known noise

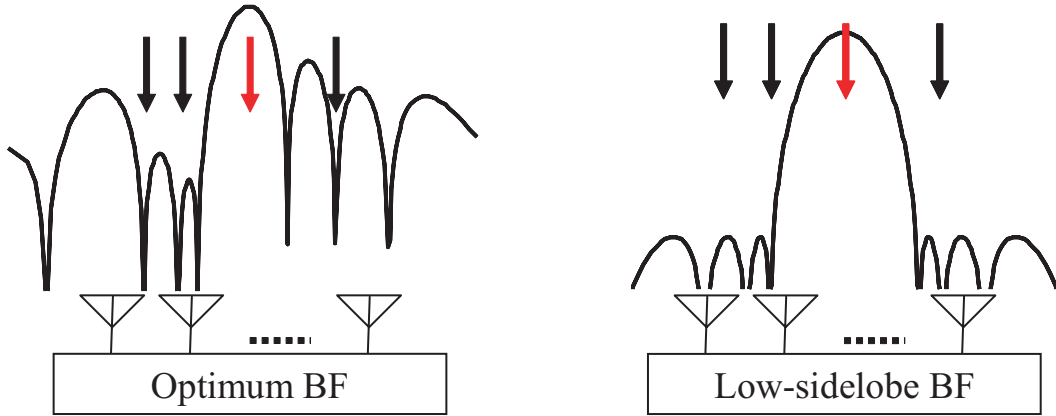


Fig. 4.2: Operations of optimum beamformer and low-sidelobe beamformer.

level enhancement effect [53]. Moreover, DCMF is extremely sensitive to the DOA estimation accuracy and a large number of snapshots is required to estimate the sample correlation matrix with high quality. However, in fact, DCMF has the tendency to miscapture the signal of interest from a small amount of DOA estimation errors; hence, the artificial noise injection technique has been studied by avoiding its unstable operation [54].

The sample data vector received at an antenna array can be modeled by the linear combination of the desired signal (subscripted by ‘0’) and the L interferers as

$$\mathbf{x}(t) = \mathbf{v}_0 s_0(t) + \sum_{l=1}^L \mathbf{v}_l s_l(t) + \mathbf{n}(t), \quad (4.1)$$

where v_i denotes the spatial signature of the signal $s_i(t)$, and $n(t)$ is an AWGN. The array output $y(t)$ is obtained as

$$y(t) = y_d(t) + y_u(t) + y_n(t). \quad (4.2)$$

The output signal components contributed by the desired signal, interferers, and noise are written as

$$y_d(t) = \mathbf{w}^H \mathbf{v}_0 s_0(t), \quad (4.3)$$

$$y_u(t) = \mathbf{w}^H \sum_{l=1}^L \mathbf{v}_l s_l(t), \quad (4.4)$$

$$y_n(t) = \mathbf{w}^H \mathbf{n}(t), \quad (4.5)$$

respectively, where \mathbf{w} is the beamforming weight vector. On the basis of the above relations, the output SINR can be obtained by

$$\begin{aligned} \text{SINR}_{\text{out}} &= \frac{P_d}{P_u + P_n} = \frac{E[|y_d(t)|^2]}{E[|y_u(t)|^2] + E[|y_n(t)|^2]} \\ &= \frac{P_0 \mathbf{w}^H \mathbf{v}_0 \mathbf{v}_0^H \mathbf{w}}{\sum_{l=1}^L P_l \mathbf{w}^H \mathbf{v}_l \mathbf{v}_l^H \mathbf{w} + \sigma_n^2 \mathbf{w}^H \mathbf{w}} \end{aligned} \quad (4.6)$$

where the desired signal power P_0 and interferers' power P_l are $E[|s_0(t)|^2]$ and $E[|s_l(t)|^2]$, respectively. Further, additive noise is assumed to be spatially white as $E[\mathbf{n}(t)\mathbf{n}^H(t)] = \sigma_n^2 \mathbf{I}$. Adaptive beamforming in smart antenna systems usually improves the SINR performance by selecting the optimum weight vector based on the following criteria.

ZF (Zero-forcing)

The optimum weight can be determined by the deterministic maximum likelihood waveform estimator [1, 53], which is referred to as ZF in this paper. The ZF technique can combine the output signal retaining the desired signal output by unit gain and suppressing all interference components completely by forcing zeros as

$$\begin{aligned} \mathbf{w}^H \mathbf{v}_0 &= \mathbf{v}_0^H \mathbf{w} = 1 \\ \mathbf{w}^H \mathbf{v}_1 &= \mathbf{v}_1^H \mathbf{w} = 0 \\ &\vdots \\ \mathbf{w}^H \mathbf{v}_L &= \mathbf{v}_L^H \mathbf{w} = 0 \end{aligned}, \quad (4.7)$$

and the matrix notation is given by

$$\mathbf{V}^H \mathbf{w} = \mathbf{g}. \quad (4.8)$$

where \mathbf{g} is a gain vector typically given by $[1, 0, \dots, 0]^T$. Using Moore-Penrose's matrix inversion [2], the optimum weight vector with minimum norm can be determined as

$$\mathbf{w}_{\text{ZF}} = \mathbf{V}^{(+)} \mathbf{g}, \quad (4.9)$$

where

$$\mathbf{V}^{(+)} = \mathbf{V}(\mathbf{V}^H \mathbf{V})^{-1}. \quad (4.10)$$

DCMP (Directional Constrained Minimizing Power)

The DCMP beamformer minimizes the output power under the constraint condition as

$$\begin{aligned} \arg \min_{\mathbf{w}} (P_{out} = \mathbf{w}^H \mathbf{R}_{xx} \mathbf{w}) \\ \text{subject to } \mathbf{C}^H \mathbf{w} = \mathbf{g} \end{aligned}, \quad (4.11)$$

where $\mathbf{C} \in \mathbb{C}^{M \times L}$ is a directional constraint matrix and $\mathbf{g} \in \mathbb{C}^{M \times 1}$ is a gain vector, which often becomes the desired signal vector \mathbf{v}_0 ($\in \mathbb{C}^{M \times 1}$) and scalar value (typically chosen by unit gain), respectively, if a single constraint for the desired signal is applied. The optimum weight vector for the DCMP criteria can be determined by the Lagrange multiplier method as

$$\mathbf{w}_{\text{DCMP}} = \left(\frac{1}{\mathbf{v}_0^H \mathbf{R}_{xx} \mathbf{v}_0} \right) \mathbf{R}_{xx}^{-1} \mathbf{v}_0, \quad (4.12)$$

[50].

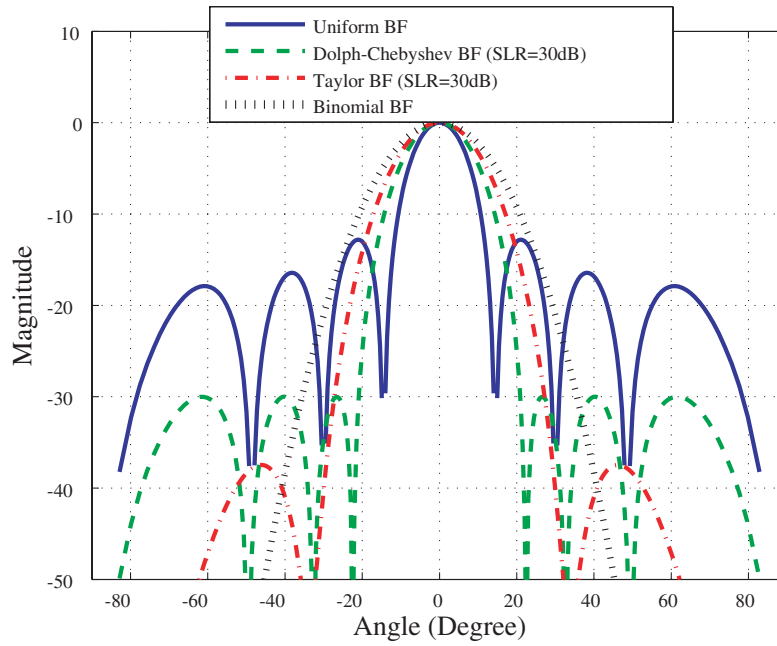


Fig. 4.3: Beam patterns weighted by various windows.

4.2.2 Low-sidelobe Beamformers

An adaptive beamformer in a smart antenna system can operate only in the presence of white noise by the quiescent beam pattern for the desired signal. In such a situation, it is not necessary for a beamformer to be adaptive with null steering capability. However, if interferences exist, the undesired power is usually received by the sidelobe of the beam pattern. In order to avoid this, it is necessary to select the beam pattern with a low sidelobe that completely suppresses the interference power. Several well-known deterministic designs, such as the Dolph-Chebyshev array, have been referred to in this study. Dolph-Chebyshev array design is a simple method for obtaining beam patterns with prescribed equi-ripple low sidelobe [51, 52]. Figure 4.3 shows various quiescent beamformers, including Dolph-Chebyshev, Taylor, and binomial windows.

In certain environments, low-sidelobe beamformers may be considered the simple and safe beamformer with sub-optimum SINR performance. They have extremely low complexities with just simple scalar amplitude weighting operation of the steering vector, which are also suitable for implementation high-speed logic devices, such as FPGAs. Due to its low complexity, application of high-speed weight adaptation capability may be very useful in various wireless communication systems for fast fading environments. In addition, an equi-ripple low sidelobe leads to good interference suppression performance in the presence of the interferences' AS. However, broadened beamwidth caused by a low-sidelobe beam pattern affects the angular resolution; hence, the SINR performance will be degraded if the source separation between the desired signal and adjacent interferers is too small for its beamwidth. Hereafter, this paper refers to the interferers existing within the beamwidth as “*in-beam*” interferer. The relationship between low sidelobe and beamwidth is an inherent trade-off.

4.2.3 Performance Comparison

Optimum beamformers, such as ZF and DCMP, have an optimum performance combining the desired signal and suppressing the interferers; however, one of the major drawbacks is the computational complexity of the matrix inversion. On the other hand, low-sidelobe beamformers have extremely low complexities. Figure 4.4 shows the normalized number of operations required to compute the weight vector in each beamformer, where the weight vectors are computed respectively by

$$\mathbf{w}_{\text{DC}} = \mathbf{C}_{\text{DC}} \odot \mathbf{v}_0, \quad (4.13)$$

$$\mathbf{w}_{\text{DCMP}} = \mathbf{R}_{xx}^{-1} \mathbf{v}_0, \quad (4.14)$$

$$\mathbf{w}_{\text{ZF}} = \mathbf{V}(\mathbf{V}^H \mathbf{V})^{-1} \mathbf{g}, \quad (4.15)$$

where \mathbf{C}_{DC} and \odot denote the Dolph-Chebyshev tapering window coefficients and the element-wise multiplication operator, respectively. The computation load of ZF depends on the number of sources while those of DC-BF and DCMP are constant. In this comparison, only the operations for the weight computation are counted and it is assumed that the data, such as the correlation matrix and the spatial signatures of the sources \mathbf{v} , are already known. It can be seen that the Dolph-Chebyshev beamformer has great advantage of the computation load comparing with those of the optimum beamformers.

In general, the optimum beamformers and low-sidelobe beamformers have different performances depending on the separation angles between the desired signal and the interferer. Eq.(4.7) can be rewritten using a spatial correlation coefficient between the spatial signature of signals and the weight vector by

$$\text{SINR}_{\text{out}} = \frac{P_0 |\mathbf{v}_0|^2 |\beta_0|^2}{\sum_{l=1}^L P_l |\mathbf{v}_l|^2 |\beta_l|^2 + \sigma_n^2}, \quad (4.16)$$

where the spatial correlation coefficient is

$$\beta = \frac{\mathbf{w}^H \mathbf{v}}{\sqrt{\mathbf{w}^H \mathbf{w}} \cdot \sqrt{\mathbf{v}^H \mathbf{v}}}. \quad (4.17)$$

Figure 4.5 displays the characteristics of the correlation coefficient β , which refers to the contribution on the output signal ('1' implies fully contributive and '0' implies no contribution). The subscripted β_{user} and β_{intf} are used for the desired signal and interferer, respectively. This simulation assumed that the planar waves, including single desired signal (located at 0° , broadside) and single interference (located at $0^\circ \sim 90^\circ$), arrived at an 8-element ULA (uniform linear array) antenna; the weight vector was determined by their DOAs. The optimum beamformers, including ZF and DCMP, simultaneously operate the beamforming and nullsteering. However, the uniform beamformer (U-BF) and low-sidelobe DC-BF only perform beamforming for the desired signal. The beamforming performance in the optimum beamformers with small source

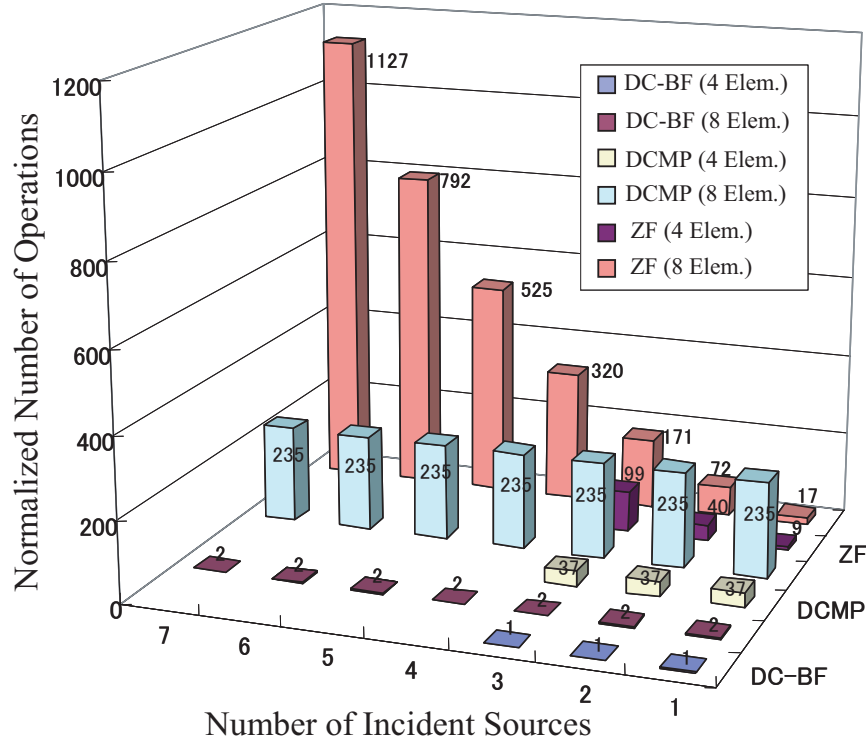


Fig. 4.4: Computation load comparison; normalized number of operations.

separation within the beamwidth¹ are significantly degraded. This is because an excessive interference rejection constraint leads to an unintentional shift of the mainlobe place. On the contrary, the interference's power usually appears in the output signal in the U-BF and DC-BF to degrade the SINR characteristic in the small source separation within the beamwidth. This is because the interference rejection capability is not supported in such beamformers.

The performance of the adaptive beamformers is usually assessed by the SINR characteristics. Figure 4.6 shows the SINR characteristics when the SNR at every element is 10 dB. Theoretically, an optimum SINR of 19 dB can be achieved by beamforming with an 8-element antenna ($10 + 10 \log_{10} 8 = 19$ dB) if the interference's power is perfectly eliminated. The SINR of U-BF has an optimum performance only when the interferer is located at null places on the beampattern; otherwise, it is degraded by the interference reception by the sidelobe. The DC-BF has a sub-optimum SINR performance that is slightly lower (approximately 1 dB) than the optimum performance with sufficient source separation. However, as mentioned above, broadened beamwidth caused by low-sidelobe beampattern decreases the angular resolution². In other words, if the source separation between the desired and adjacent interferer is small for its beamwidth, the SINR performance will be significantly degraded to a level less than that of the optimum beamformers.

¹It means the beamwidth between the first null places in the uniform beampattern (around $2 \times 13^\circ$)

²The DC-BF has sub-optimum performance due to the gap of the correlation coefficient β_{user} , as shown in Fig.4.5.

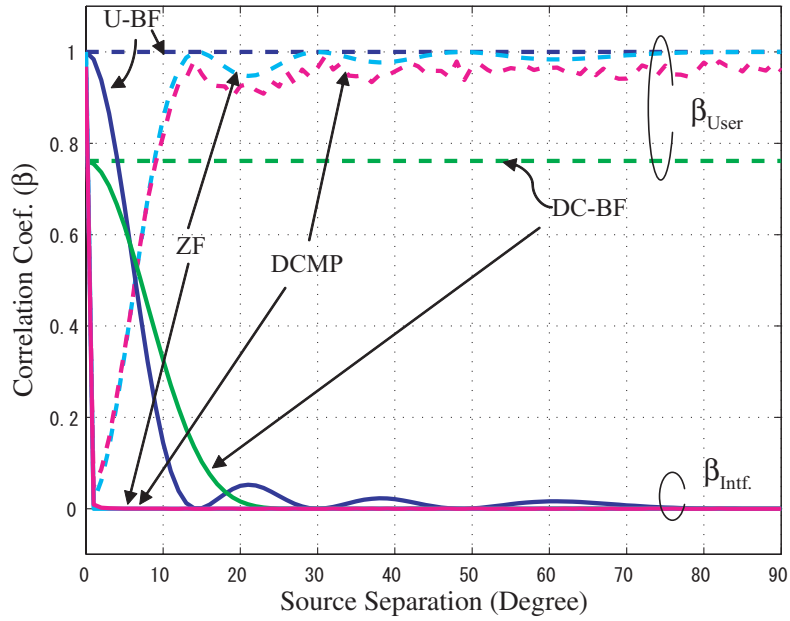


Fig. 4.5: Correlation coefficient β depending on source separation, where the desired signal arrives at 0° , broadside, and the interferer is located at $0^\circ \sim 90^\circ$ (8-element ULA).

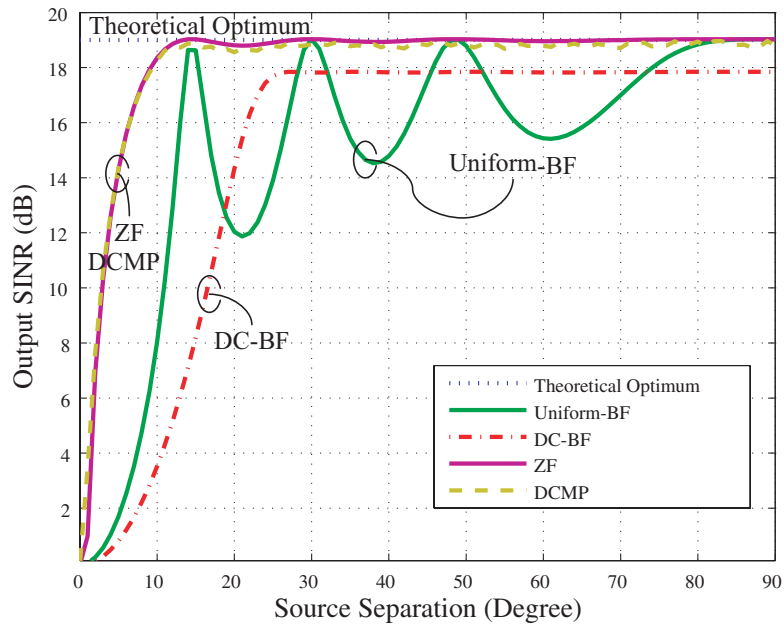


Fig. 4.6: SINR characteristics depending on source separation (8-element ULA, input SNR @ single element = 10 dB).

4.3 Null Steering Beamformer with Notch Beams

This paper proposes a novel beamforming technique with extremely low complexity. This is based on the beamforming technique with the low-sidelobe beampattern using Dolph-Chebyshev tapering window. The optional null-steering processing provides in-beam interference rejection capability with extremely low computation complexity, thus the SINR degradation can be decreased.

4.3.1 Basic Principle

It basically steers the mainlobe toward the user direction and completely suppresses the interferers by low sidelobe with the Dolph-Chebyshev beampattern. The low-sidelobe beamformer has the significant advantage of low complexity without huge computation load in optimum techniques, such as ZF and DCMP for explicitly nullifying interferences. However, if certain interferers exist within the broad mainlobe area (*in-beam*), the performance will be considerably degraded because of unavoidable interference reception. In this system, the interferers within the mainlobe can be canceled out by optional null-steering processing with a notch beampattern. The final beamforming weight is computed by simple convolution operations of pre-computed Dolph-Chebyshev beam and optional canceling beams of notch beams; hence, the computation load for weight generation is very small.

The Dolph-Chebyshev beam is usually used for beamforming toward the user DOA. The interferers are totally suppressed by a low sidelobe. The low-sidelobe beamformer, such as the DC-BF, does not require time-consuming tasks such as the inversion of the complex valued correlation matrix. However, the reception of the interferers' power in a low sidelobe is not zero; hence, the SINR performance is not optimum, as mentioned above. Further, if an interferer exists within the broadened mainlobe area, the low-sidelobe beamformer cannot suppress the interferers any more. This paper proposes the cascade beamformer of a low-sidelobe DC beam and optional canceling beams in order to overcome this; this is termed Null-steering Dolph-Chebyshev Beamformer (NDC-BF). In NDC-BF, the beamformer adaptively performs beamforming for user signal and nullsteering only for the in-beam interferers with independent nulls as

$$\mathbf{w}_{\text{null}}^H \hat{\mathbf{v}}_l = 0, \quad (4.18)$$

and $\bar{\mathbf{w}}_{\text{beam}}$ is a low-sidelobe beam determined by Dolph-Chebyshev tapering window \mathbf{C}_{DC} , denoted by

$$\bar{\mathbf{w}}_{\text{beam}} = \mathbf{C}_{DC} \odot \hat{\mathbf{v}}_0, \quad (4.19)$$

where $\hat{\mathbf{v}}_0$ and $\hat{\mathbf{v}}_l$ are the estimated spatial signature vectors of user and interferers, respectively, by DOA estimation pre-processing. Figure 4.7 shows the cascade beamforming structure consisting of the beamforming stage and optional post null-steering stage for a single null. Regarding digital signal processing, the total beamforming weight can be computed immediately

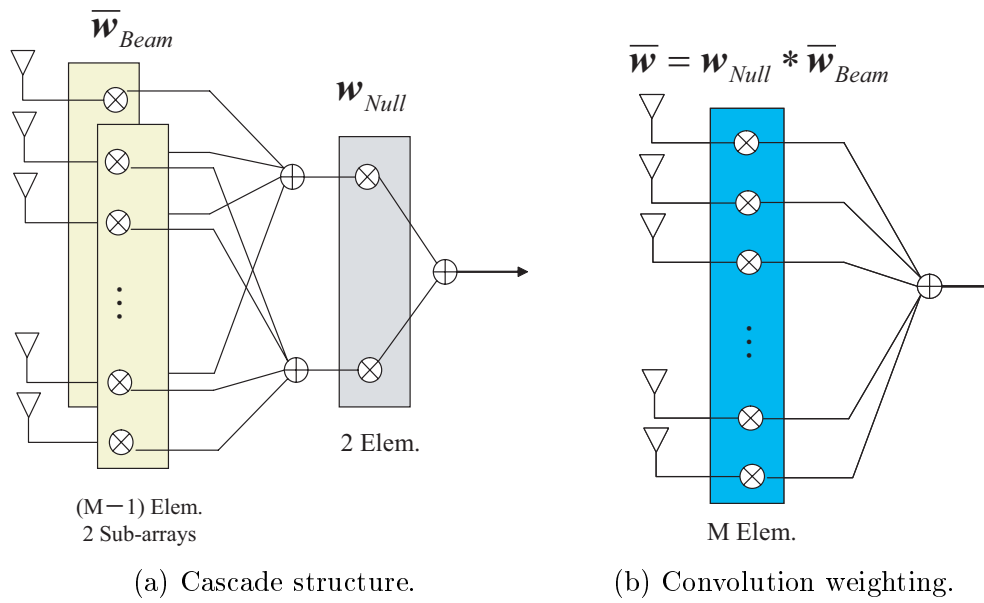


Fig. 4.7: Cascade beamforming structure (single null).

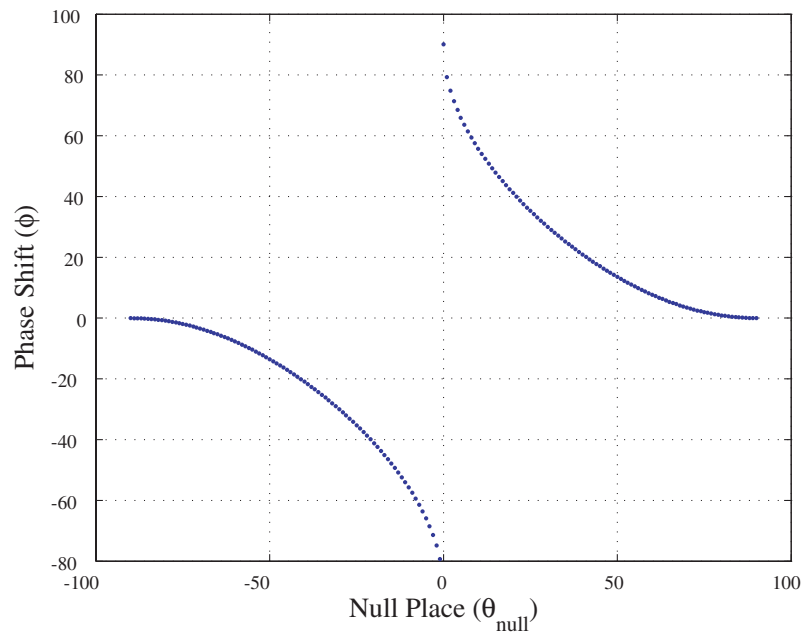
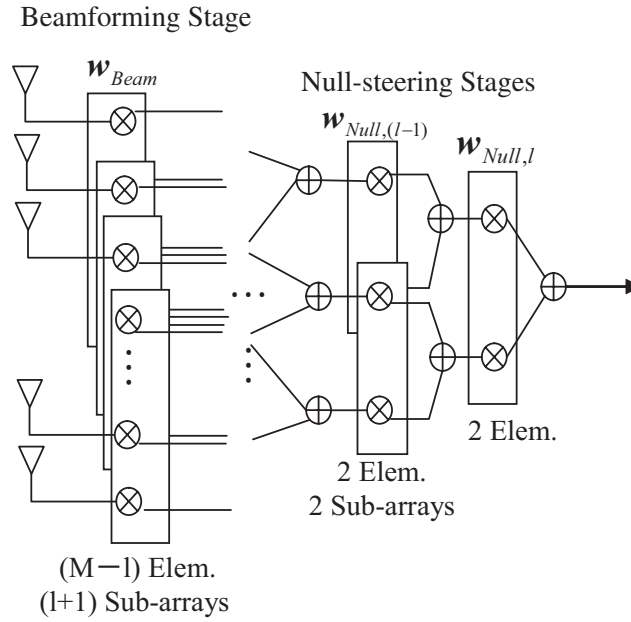


Fig. 4.8: Relationship between desired null place and required phase shift.


 Fig. 4.9: Generalized cascade beamforming structure (l nulls).

by element space convolution instead of physically cascaded structure [55] as

$$\mathbf{w}_{\text{NDC-BF}}^T = \bar{\mathbf{w}}_{\text{beam}}^T * \mathbf{w}_{\text{null}}^T, \quad (4.20)$$

where $*$ denotes convolution operation and $\bar{\mathbf{w}}_{\text{beam}} \in \mathbb{C}^{(M-l) \times 1}$, $\mathbf{w}_{\text{null}} \in \mathbb{C}^{2 \times 1}$. The notch beam to nulling the power in the direction θ_{null} is computed as

$$\mathbf{w}_{\text{null}} = \left[1, e^{-j\pi \sin \phi} \right]^T, \quad (4.21)$$

where

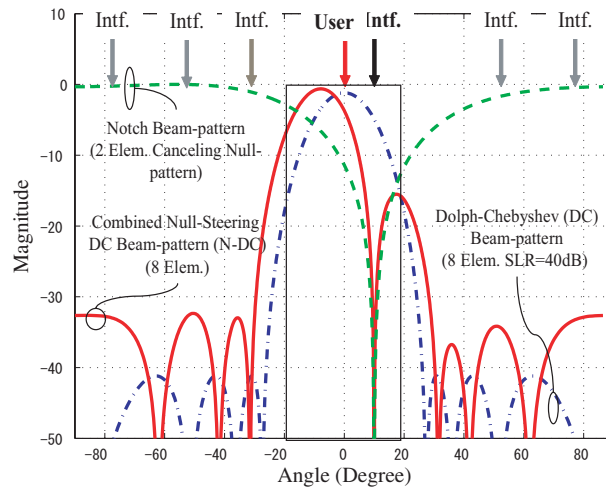
$$\phi = \begin{cases} \sin^{-1} [1 - \sin \theta_{\text{null}}] & 0 \leq \theta_{\text{null}} < \pi/2 \\ -\sin^{-1} [1 + \sin \theta_{\text{null}}] & -\pi/2 \leq \theta_{\text{null}} < 0 \end{cases}, \quad (4.22)$$

and the relationship between the phase shift ϕ and null-steering direction θ_{null} is illustrated in Fig. 4.8.

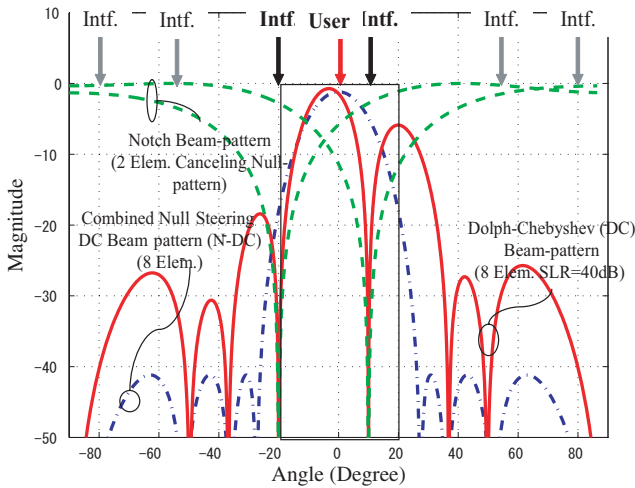
Figure 4.9 shows a generalized version of the cascade structure for the M -element array comprising the beamforming stage and $l (< M - 1)$ optional post null-steering stages with notch beams. The weight vector can be extended by

$$\mathbf{w}_{\text{NDC-BF}}^T = \bar{\mathbf{w}}_{\text{beam}}^T * \mathbf{w}_{\text{null},1}^T * \cdots * \mathbf{w}_{\text{null},l}^T. \quad (4.23)$$

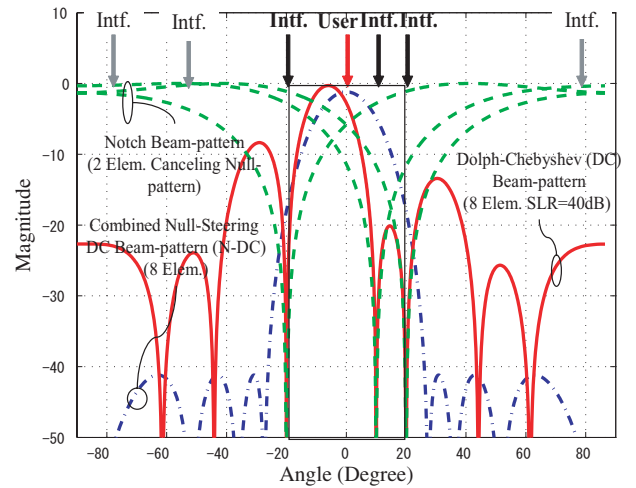
Figure 4.10 shows the examples of some beamforming scenarios with multiple null steering stages to reject the in-beam interferers within the mainlobe when there exist seven interferers; one (Fig.4.10(a)), two (Fig.4.10(b)), and three (Fig.4.10(c)) are in-beam interference(s) within the mainlobe area. The user DOA is set by 0° and the in-beam interferers are located at 10° , -20° and 20° . The in-beam interferences are observed to be effectively eliminated by



(a) Single null (in-beam intf @ 10°).



(b) Two nulls (in-beam intfs @ 10° and -20°).



(c) Three nulls (in-beam intf @ 10° , -20° and 20°).

Fig. 4.10: Beamforming scenarios in null-steering Dolph-Chebyshev beamformer (NDC-BF) with multiple nulls.

notch beams; however, the mainlobe is slightly shifted off the user direction. In addition, null-steering processing leads to an increase in the sidelobe level. Therefore, the number of independent nulls for the in-beam interferers may be limited by three or less interferers in 8-element array configuration. The performance improvement and limitation of NDC-BF will be discussed in the next subsection.

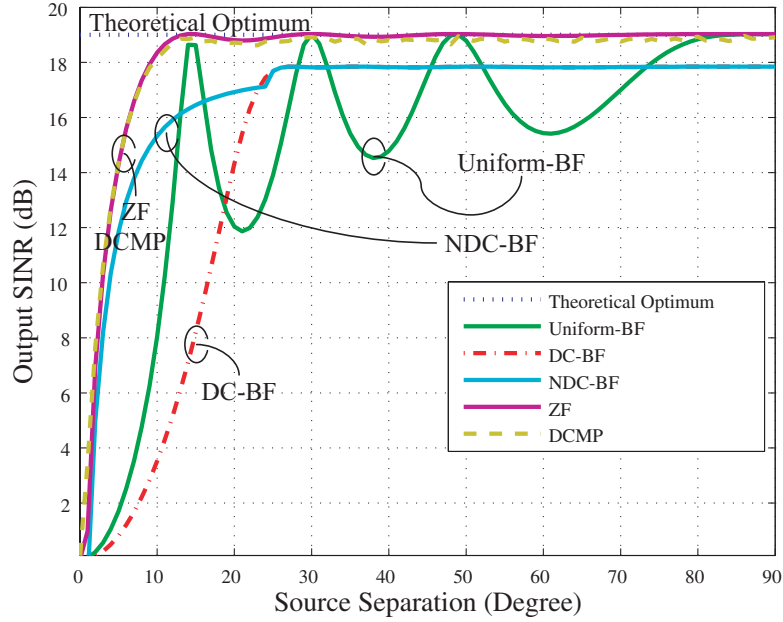


Fig. 4.11: SINR characteristics depending on source separation (8-element ULA, input SNR @ single element = 10 dB).

4.3.2 Performance Improvement and Limitation

Assuming there are no in-beam interferers without an optional null-steering stage, the proposed NDC-BF will have the same performance to that of the DC-BF. However, the SINR performance in a small source separation condition is dramatically improved, as shown in Fig.4.11. The optional null-steering stage was applied only when the source separation is below 25° (in-beam area) because the interference suppression by the low sidelobe has slightly better SINR characteristics than the optional null-steering process of the in-beam area.

The computation complexity, involved in NDC-BF is greatly low than that of the other optimum beamformers. Table 4.1 presents the computational complexity for the K -element ULA antenna in the presence of L sources. In NDC-BF, the multiplications and additions required for Eq.(4.20) were counted in each case assuming that the DC beams and notch beams were precomputed and stored in the ROM. The complexity of the DCMP in Eq.(4.14) can be computed based on the fact that the linear algebraic solution, including LU decomposition ($K^3/3$), forward substitution ($K^2/2$), and backward substitution ($K^2/2$), takes a total of $(K^3/3+K^2)$ executions of complex multiplications and additions [97]. Similarly, the complexity of ZF in Eq.(4.15) can be computed based on the fact that the matrix inversion including LU decomposition ($K^3/3$), forward substitution ($K^3/6$), and backward substitution ($K^3/2$) takes a total of (K^3) executions of complex multiplications and additions [97]. As shown in Tab.4.1, the execution number of real operations are obtained as four times those of complex operations. Figure 4.12 shows the comparison between the computational complexity in the cases of 4 and 8 antenna elements, where no operations are required for NDC-BF in the presence of the

Table 4.1: Computational load for weight computation in real operations (K elements, L sources).

	Multiplications	Additions	Total operations
NDC-BF (single null)	$8(K - 1)$	$2K$	$10K - 8$
NDC-BF (two nulls)	$12(K - 2) + 4$	$4K + 2$	$16K - 18$
NDC-BF (three nulls)	$16(K - 3) + 12$	$6K + 6$	$22K - 30$
DCMP	$\frac{4}{3}K^3 + 4K^2$	$\frac{4}{3}K^3 + 4K^2$	$\frac{8}{3}K^3 + 8K^2$
ZF	$8L^2K + 4L^3$	$8L^2K + 4L^3$	$16L^2K + 8L^3$

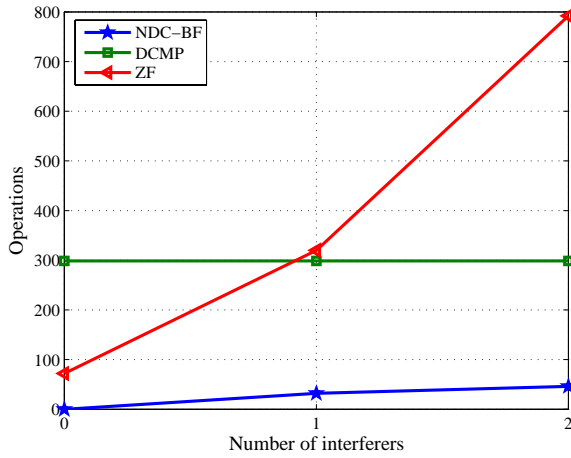
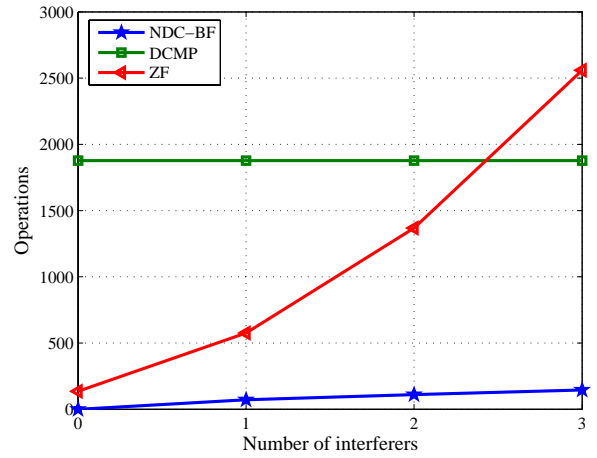
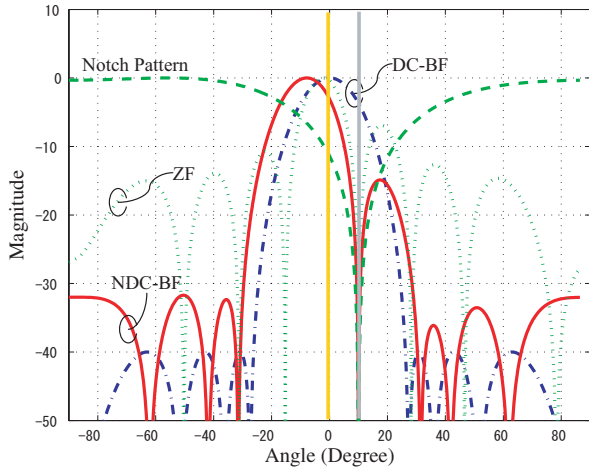
(a) $K = 4$ elements.(b) $K = 8$ elements.

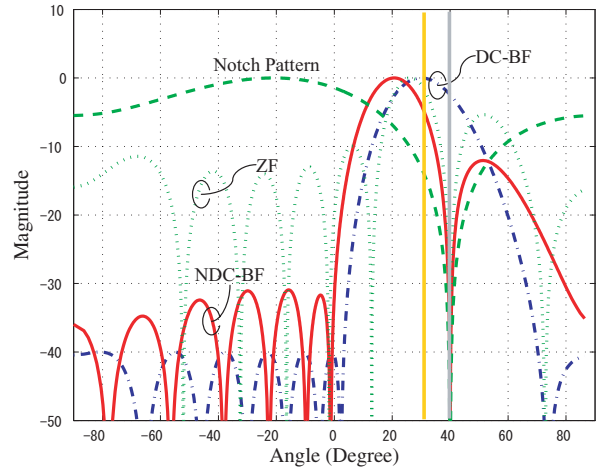
Fig. 4.12: Computational load comparison.

desired signal only because it refers to the precomputed beampattern for the desired signal in the ROM. It is clarified that the proposed NDC-BF has extremely low complexity.

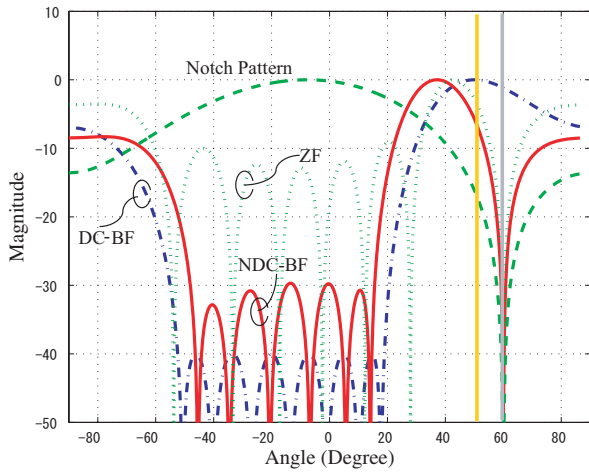
On the other hand, the mainlobe is slightly shifted off the user direction by eliminating the in-beam interferences with notch beams. Thus, the receive level for the user signal is usually dropped unavoidably. Fig.4.13 shows certain typical beampatterns of NDC-BF and ZF at different angles where the source separation is 10° . In fact, the level drop caused by the mainlobe shift also appears in the ZF beamformer; however, it is less than that of NDC-BF. This is because ZF optimizes SINR by simultaneously applying constraints for both the mainlobe and nulls while NDC-BF places nulls independent of the mainlobe. Further, the number of nulls is typically limited to three or less for an 8-element antenna array.



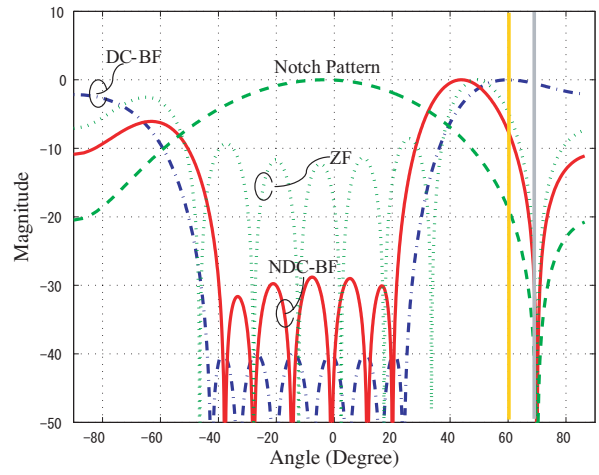
(a) user = 0° , interferer = 10°



(b) user = 30° , interferer = 40°



(c) user = 50° , interferer = 60°



(d) user = 60° , interferer = 70°

Fig. 4.13: Angle dependency of mainlobe in NDC-BF, where the source separation is 10° .

Table 4.2: FPGA resources.

LEs	1,269 (about 30,000 equiv. gates)	
ROM	DC-beam	2,064 words ($129 * 8 * 2$)
		1,792 words ($129 * 7 * 2$)
		1,536 words ($129 * 6 * 2$)
		1,280 words ($129 * 5 * 2$)
	Notch-beam	258 words ($129 * 1 * 2$)
	Total bits	83,160 bits ($6,930 \text{ word} * 12 \text{ bits}$)
MACs	18 ($16 * 12$ MACs)	
Clock Freq.	119 MHz	
Required clocks	$< 30 + N_{\text{frame}}$	

4.4 Hardware Implementation

The significant feature of NDC-BF is low complexity without a huge computation load in the case of optimum techniques, such as ZF and DCMP, for explicitly nulling interferences although the SINR performance is not optimum. Figure 4.14 shows the computation flow of this system, where we can place nulls at desired locations by simple operations; thus, the interferers within the mainlobe can be canceled by optional null-steering processing with notch beams, which are pre-computed and stored in the ROM in the FPGA's embedded memory block. The final beamforming weight is computed by the simple convolution operation of the pre-computed DC beam and optional canceling beams; hence, the computation load for weight generation is very small. In the case of the single null, this operation requires only two scalar multiplications and one vector addition. Therefore, fast weight generation can be realized without additional complexity. The block diagram for NDC-BF on FPGA is shown in Fig.4.15. The DC beams and notch beams are pre-computed and stored in the ROM. According to the DOA estimation results in pre-processing, the simple convolution operation of the pre-computed weights can be performed easily. NDC-BF consists of ROMs for the pre-computed beams, two-tap complex FIR filter for convolution operation, and complex multipliers for beamforming. The precision of the DC beams and notch beams are appropriately chosen as 12 and 8 bits, respectively. A minimum precision of 8 bits for DC beams and notch beams is required for a reasonable performance in fixed-point beamforming, as shown in Fig.4.16, where (a) and (b) show the fixed-point effect on beamwidth and the sidelobe level of DC beam, respectively and (c) and (d) show the fixed-point effect on null-width and null-depth of notch beam, respectively.

The FPGA implementation results are shown in Tab.4.2. According to the results, approximately 30,000 logic gates were used and 83,160 memory bits were required. Beamforming is computed extremely fast in parallel using 16 MACs. The associated time for weight generation and beamforming is, for example, approximately $1.4\mu\text{s}$, assuming that the frame length N_{frame} is 136 in the three-null case.

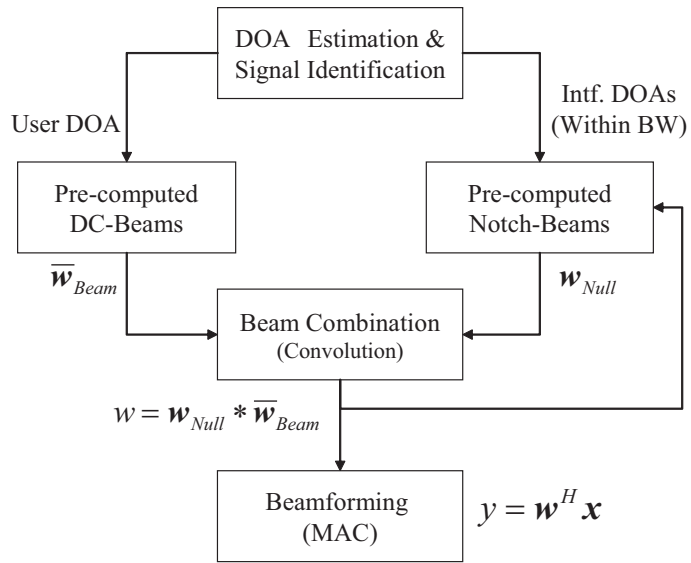


Fig. 4.14: Computation flow of NDC-BF.

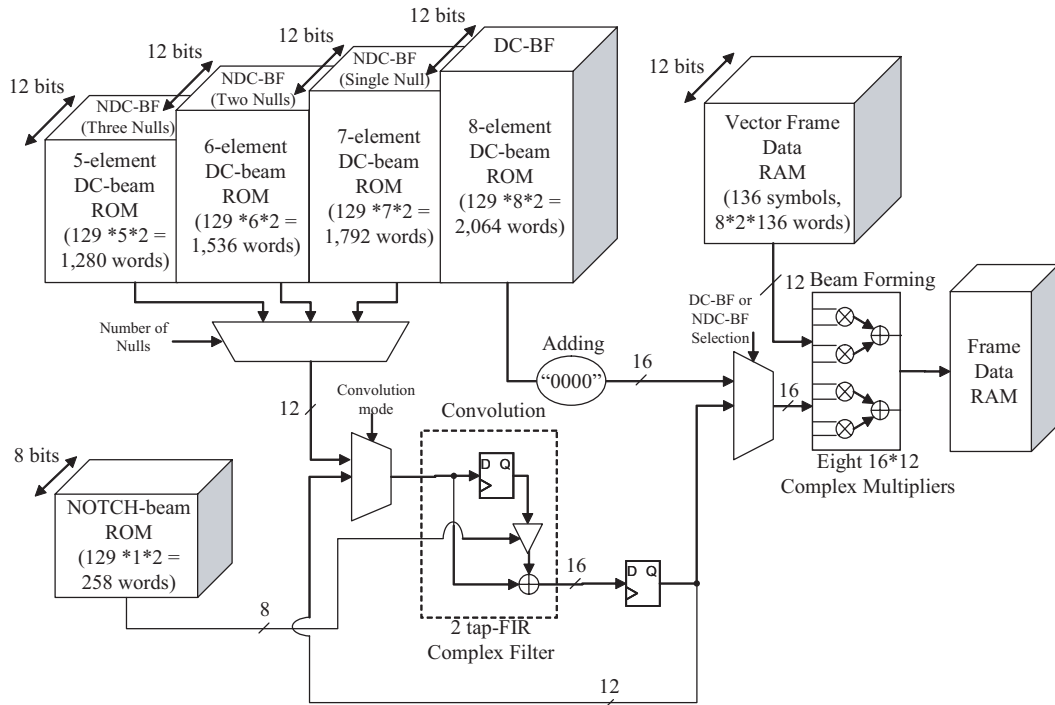
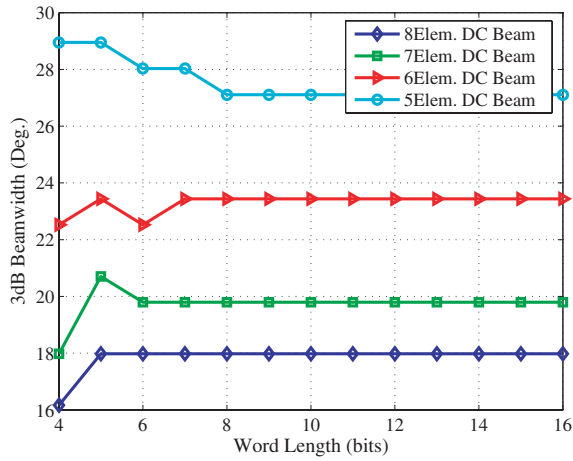
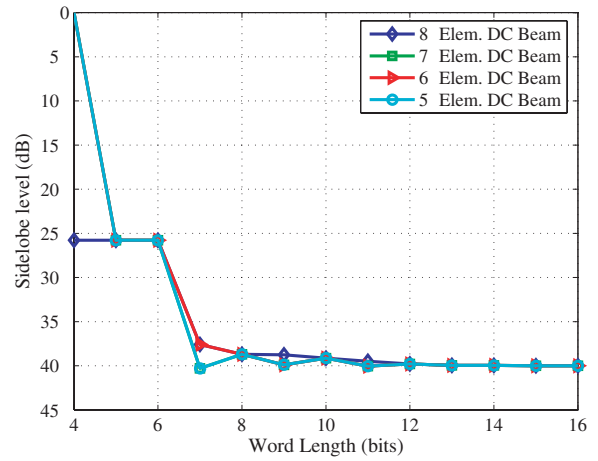


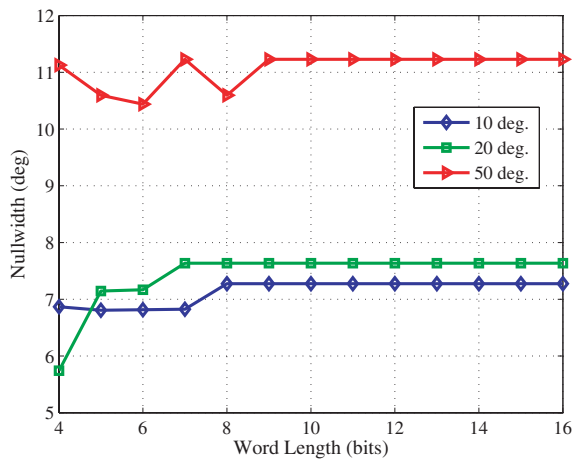
Fig. 4.15: DSP Block Diagram for NDC-BF



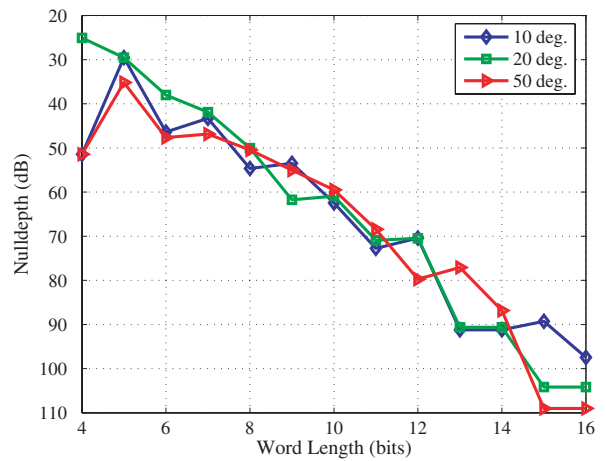
(a) 3dB Beamwidth.



(b) Sidelobe Level (-40 dB).



(c) Null width @ -20dB.



(d) Null depth.

Fig. 4.16: Characteristics of main beam and notch beam with fixed wordlength.

4.5 Performance Evaluation by Computer Simulations

This section evaluates the performance of the proposed NDC-BF through computer simulations in certain cases.

In the case of an urban cellular uplink channel, the BER (bit error rates) performance of the proposed NDC-BF is first discussed for both the LOS and multipath models. It was assumed that four waves, including single user and three interferers (two of them being in-beam interferers), arrived at the half wavelength equi-spaced 8-element antenna array; their DOAs are perfectly estimated. Figure 4.17 shows the schematic simulation configuration. The detailed parameters are also listed in Tab.4.3. The performances of the conventional uniform beamformer (U-BF), low-sidelobe DC-BF, and ZF are also simulated for comparison with the proposed system. While the planar wave model without fading was assumed in the LOS environment the Rayleigh fading model with a small AS was considered in the multipath environment. In an urban cellular environment, the time delays among the sub-paths can be neglected. Thus, the spatial signature for the i -th source is approximately given by

$$\mathbf{v}_i = \sum_{j=1}^{N_i} \beta_{ij} \mathbf{a}(\theta_i + \tilde{\theta}_{ij}), \quad (4.24)$$

where

- β_{ij} : Complex amplitude with Rayleigh distributed magnitude of j -th scattered sub-path
- θ_i : Nominal DOA for i -th source
- $\tilde{\theta}_{ij}$: DOA deviation of j -th sub-path of Gaussian random variable $\sim \mathcal{N}(0, \sigma_{\theta_i}^2)$
- N_i : Number of sub-paths for i -th source

[40] and the AS $2\sigma_{\theta_i}$ for each source was set by 3° .

Figures 4.18 and 4.19 illustrate the BER performances in LOS and multipath environments, respectively. The average INR (Interferer to Noise Ratio) of each interferer was set as 9 dB. Except for DOA estimator, in order to evaluate only the beamformer, the information of the source locations was assumed to be perfectly known, as mentioned above. In the previous section, the SINR characteristics of the NDC-BF were not optimum; hence, they were inferior to those of optimum beamformers such as ZF. However, from these results, it is clear that the proposed system performance is comparable to the ZF technique under the BER criteria, and the computation load is extremely low. For example, an 8-element NDC-BF with two nulls requires only three scalar \times vector multiplications and two vector summations. If the operations are counted, the computation load was approximately several tens greater than that of ZF, as mentioned in the previous section.

In order to determine the appropriate word-length for the DC beam and notch beam, the fixed-point effect was examined, as shown in Fig.4.20, where (a) and (b) show the fixed-point effect on BER performance and SINR, respectively. Simulation conditions similar to those in Tab.4.3 were applied. It can be clarified that 12- and 8-bit precisions for the DC beam and notch beam, respectively is sufficient to avoid performance degradation. Hence, the system was actually implemented with this precision.

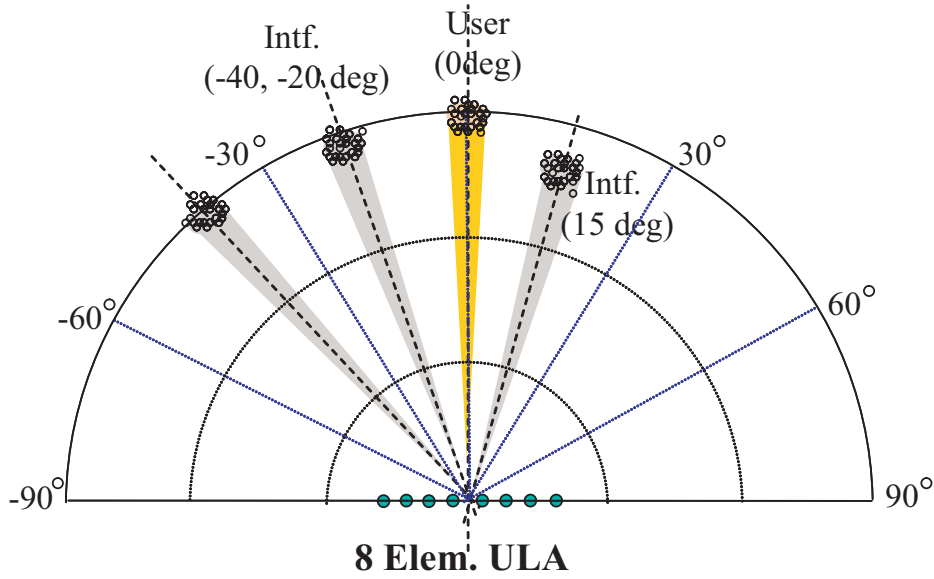


Fig. 4.17: Simulation configuration; AS=3°.

Table 4.3: Simulation parameters.

Antennas	8-Element ULA ($\lambda/2$)	
DOA Estimator	Perfect Estimation	
Beamformers	U-BF, DC-BF with SLR=40dB, NDC-BF with SLR=40dB, ZF	
Transmitting Signal	$\pi/4$ -DQPSK	
Burst Frame Length	136 Symbols (272 bits)	
Signal Sources	User	0°
	Interferers	-20, 15° (In-Beam), -40° (Out-of-Beam) Average INR @ single antenna of each signal is 9 dB
Channels	LOS (AWGN) and Multipath (Rayleigh Fading with AS = 3°, $N_i = 30$)	
Doppler Freq.	0 (Burst Stationary)	
Trials	2000	

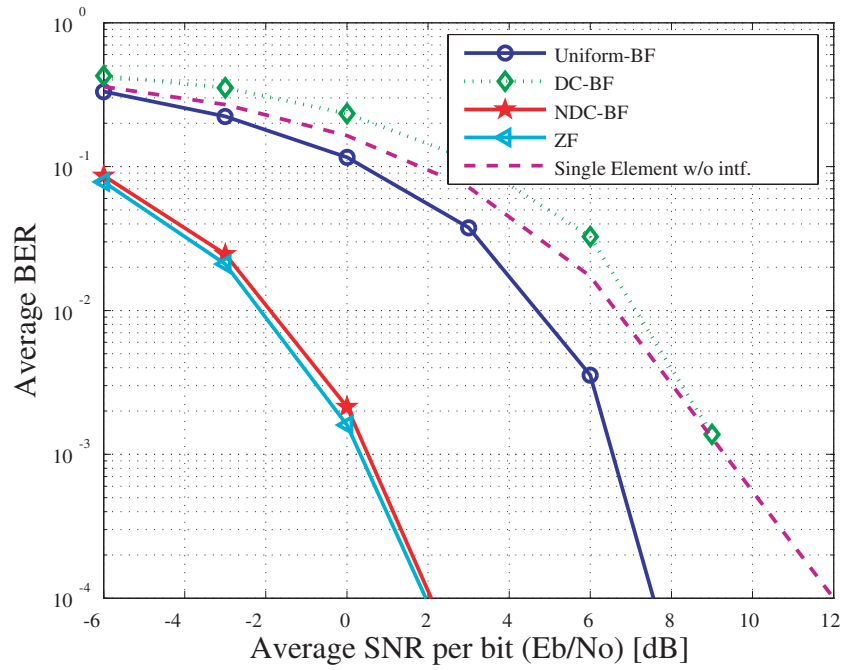


Fig. 4.18: BER performance in noise channel under plane wave assumption (LOS model).

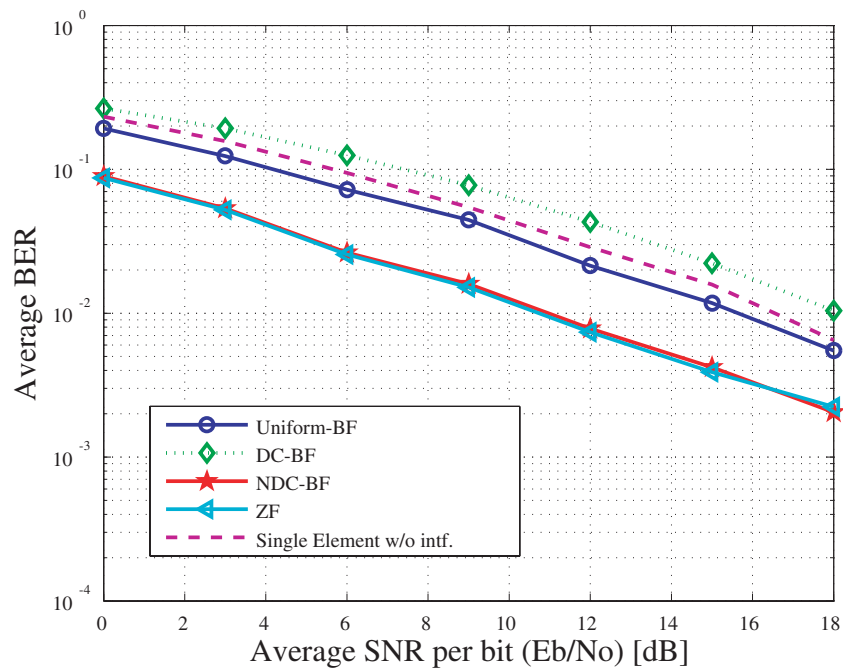
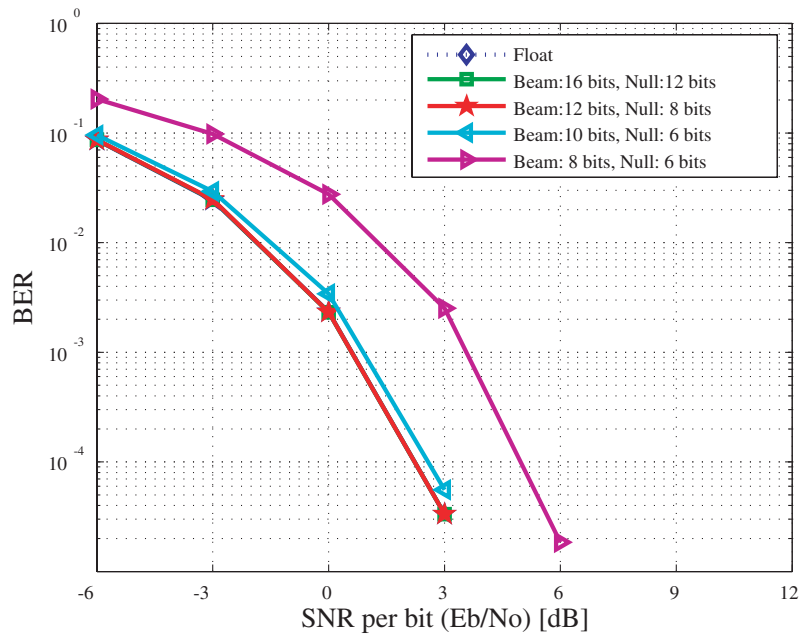
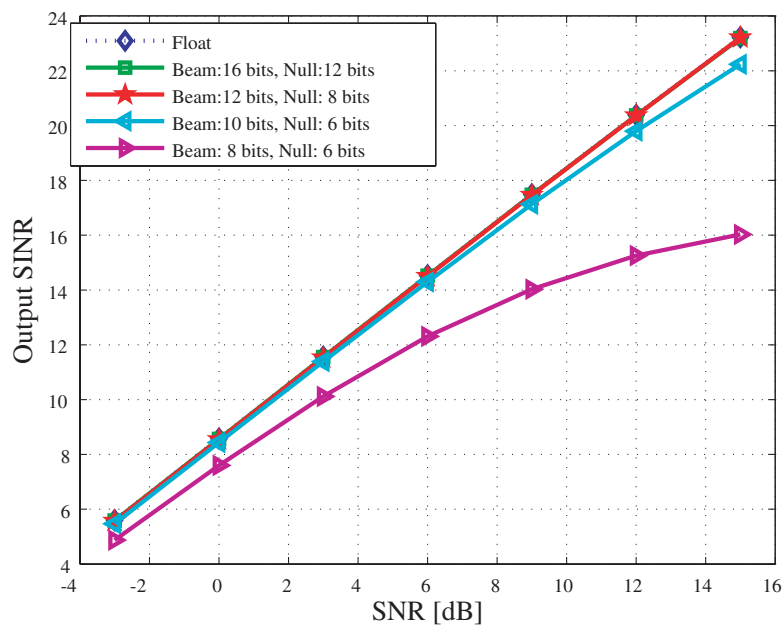


Fig. 4.19: BER performance in multipath channel under Rayleigh fading assumption (multipath model).



(a) BER performance.



(b) SINR Characteristics.

Fig. 4.20: Performance in NDC-BF with fixed-point arithmetic.

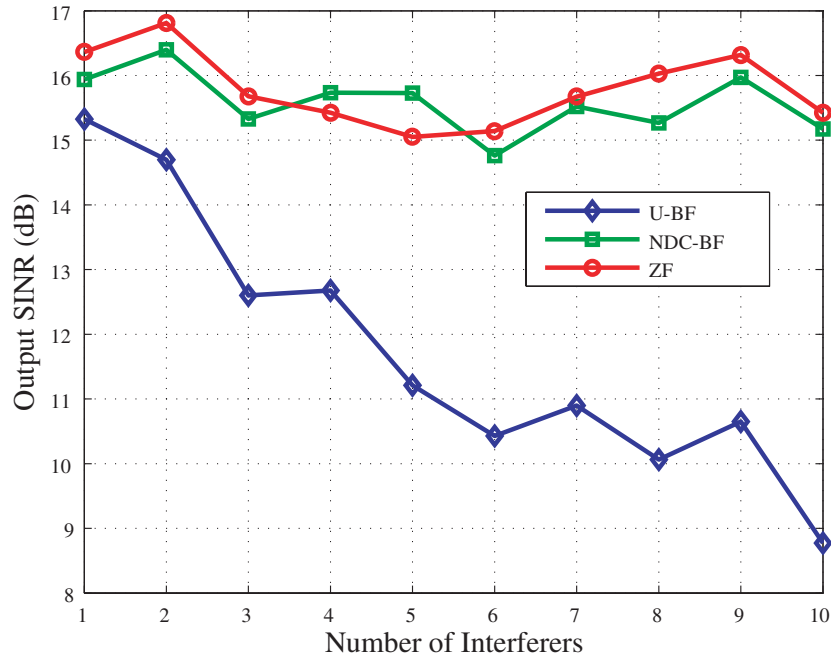


Fig. 4.21: Output SINR versus number of interferers in Rayleigh fading channel ($AS = 5^\circ$), where the DOA of the desired signal and the nearest interferer are set by 0 and 17° and the other interferers are located at $-70, -60, -50, -40, -30, 30, 40, 50, 60$ and 70° , respectively.

On the other hand, the output SINR in the presence of many interferers is discussed. Figure 4.21 shows the average output SINR performance for a number of interferences (up to 10) in Rayleigh fading channel where the AS was 5° . The DOAs of the desired signal and the nearest interferer are set as 0 and 17° respectively; the other interferers were located at $-70, -60, -50, -40, -30, 30, 40, 50, 60$, and 70° . In Fig.4.21, the output SINR was plotted adding an interferer in above sequence. All the incident signals had identical power and the other conditions were similar to those in the previous case. The result shows that conventional U-BF without adaptive null-steering or sidelobe suppression for the interferer is significantly degraded in the presence of a larger number of interferers; however, ZF and NDC-BF has an approximately flat SINR. On the basis of these results, it can be also seen that the NDC-BF will be a better choice than high-complexity optimum beamformers, such as ZF.

4.6 Summary

This paper proposes a novel beamforming technique for DOA-based smart antenna system. This system basically steers the mainlobe for the user with the Dolph-Chebyshev beam. Further, in order to avoid undesirable interference reception by broad mainlobe, an optional null-steering processing cancels the interferers within the mainlobe coverage with notch beams, which are pre-computed and stored in the ROM. This is based on a cascade structure with Dolph-Chebyshev low-sidelobe and simple notch beampatterns to cancel the in-beam interferer; however, the weight vector can be obtained by simple convolution operations of the pre-computed DC beam and optional canceling notch beams. Hence, the complexity is extremely low with such a simple weighting operation; this is suitable for implementation in high-speed logic devices, such as FPGAs. The performance improvement and limitation of the proposed beamformer was also discussed. Further, BER performances in several scenarios were assessed using computer simulations.

Chapter 5

Integrated System Evaluation

5.1 Introduction

This chapter describes an integrated system evaluation with developed hardware assuming an uplink smart antenna system that is useful for macro-cellular base stations. This system incorporates a fast DOA estimator termed UMP using the dedicated circuit device of FPGA, as presented in Chapter 3. In the case of uplink beamforming, this system basically steers the mainlobe for the user location with the beam. Further, in order to avoid undesirable interference reception by broad mainlobe, an optional null-steering processing cancels the interferers within the mainlobe coverage with notch beams. The beamforming weight is computed by a simple convolution operation of the pre-computed Dolph-Chebyshev beam and an optional canceling beam; hence, the computation load for weight generation is extremely small, as mentioned in Chapter 4.

In this chapter, the DOA estimator and beamformer are integrated on the developed testbed system that was presented in Chapter 2. Firstly, the evaluation system configuration co-designed using FPGAs and CPU will be introduced. The total integrated system will be evaluated verifying the normal operation and confirming the performance. Secondly, each processing functions are discussed according to the processing flow and the computer simulation results will be described. Some experimental results of the total performance evaluation in a radio anechoic chamber assuming LOS AWGN channel will be presented as well. Further, the problems with the calibration of antenna array and analog receivers will be discussed.

5.2 System Configuration

The integrated system consists of a DOA estimator and a beamformer, as shown in Fig.5.1. The received signals at the antenna array are downconverted into complex baseband signals and fed into the UMP DOA estimator where the DOAs of the incident signals are estimated. The UMP employs the unitary MUSIC algorithm. The NDC-BF is applied for beamforming. This basically uses the equi-ripple Dolph-Chebyshev beam with a sidelobe ratio (SLR) of 40 dB, steers the mainlobe toward the user direction, and completely suppresses the interferers by low sidelobe. Following the DOA estimation and identification, in order to eliminate in-

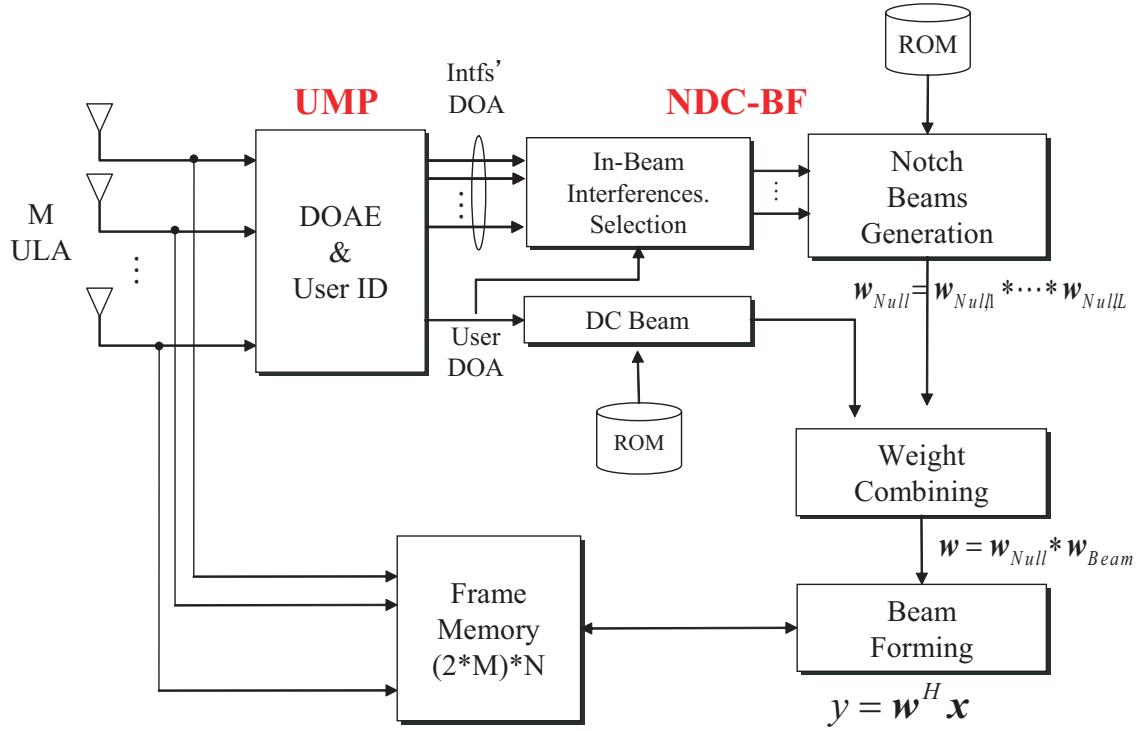


Fig. 5.1: Integrated DOA-based beamforming processing flow.

beam interferers, the interferers are classified into in-beam and out-of-beam. NDC-BF provides optional null steering processing by cascade beamforming with notch beams. The canceling beams are computed by the convolution of the pre-computed notch beams stored in the ROM. Finally, the uplink beamforming weight is combined by the convolution of the pre-computed DC beam and the canceling beam. The burst frame data is updated after beamforming with the final weight vector.

Figure 5.2 illustrates the evaluation configuration with the testbed system. It performs the DOA estimation and uplink beamforming with single FPGA (STRATIX EP1S40, Altera) and CPU (SH4, Hitachi). The FPGA has approximately 1 million equivalent gates, approximately 417 Kbytes internal memory blocks, and optimized DSP blocks [103]. CPU performs receiver calibration and synchronization tasks with software. The burst frame format is defined as shown in Fig.5.3, where a single burst consists of 136 symbols, including 16 training symbols. The modulation scheme of $\pi/4$ -shift QPSK was used.

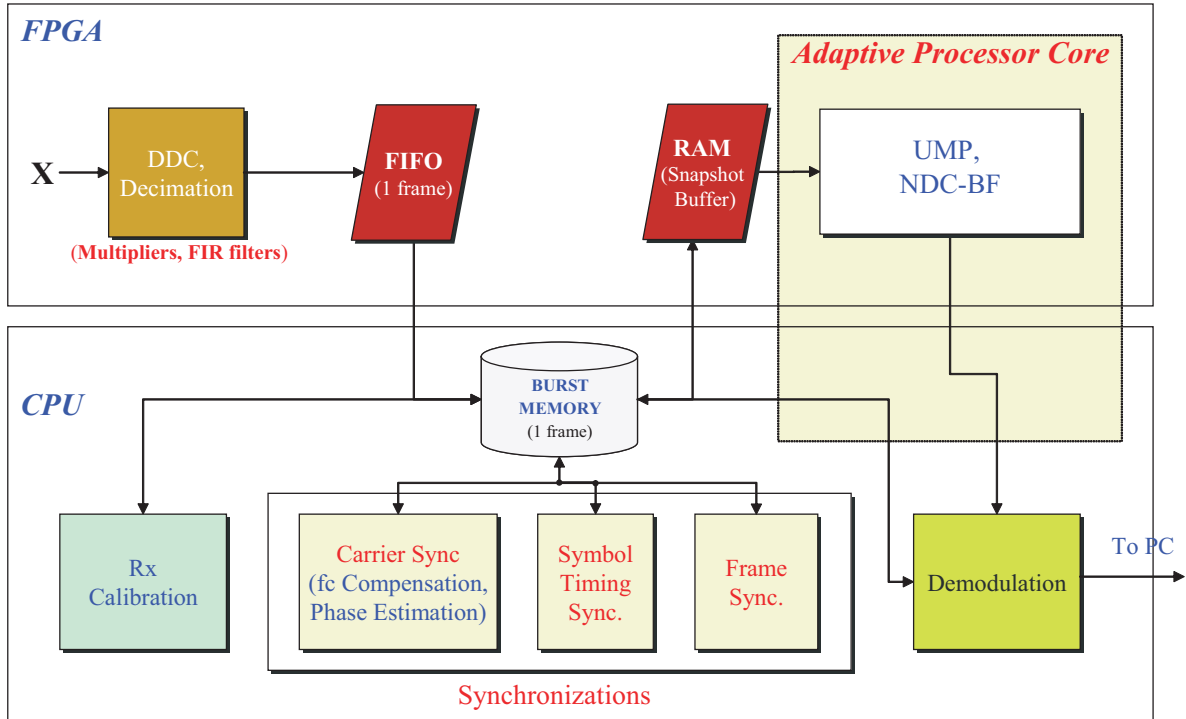


Fig. 5.2: Evaluation configuration with testbed system.

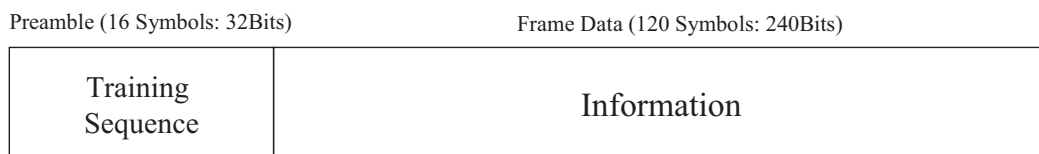


Fig. 5.3: Burst frame format.

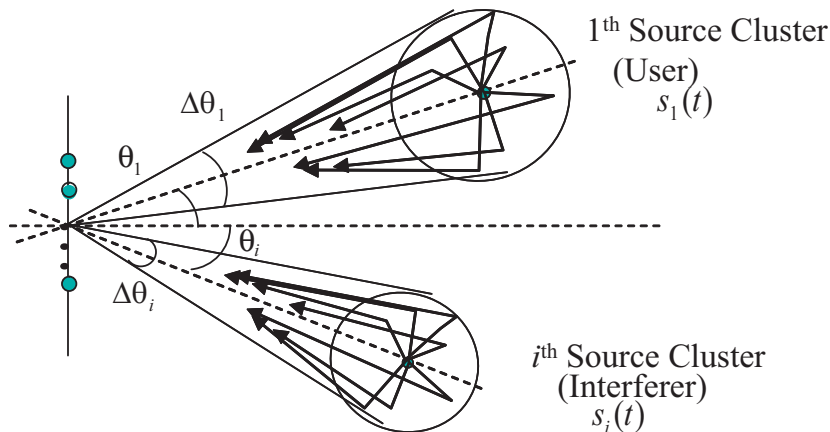


Fig. 5.4: Macro cellular channel model.

5.3 Data Model

The basic narrowband signal model was assumed in a macro cellular Rayleigh fading environment with a small AS, as shown in Fig.5.4. The transmitted signals $s_i(t)$ from the i -th source, where $i = 1, 2, \dots, L$ arrive at a M -element antenna array spaced by half-wavelength as

$$\mathbf{x}(t) = \mathbf{V} \mathbf{s}(t) + \mathbf{n}(t), \quad (5.1)$$

where the array output $\mathbf{x}(t)$ is a received data vector, and $\mathbf{s}(t)$ and $\mathbf{n}(t)$ are the signal and complex AWGN vectors, at time t , respectively. The columns of the channel matrix $\mathbf{V} = [\mathbf{v}_1, \mathbf{v}_2, \dots, \text{and } \mathbf{v}_L]$ consist of the spatial channel vectors for L sources. In the case of the i -th source cluster, the spatial channel vector \mathbf{v}_i is modeled by

$$\mathbf{v}_i = \sum_{j=1}^{N_i} \beta_{ij} \mathbf{a}(\theta_i + \tilde{\theta}_{ij}), \quad (5.2)$$

where

$$\mathbf{a}(\theta) = [1, e^{-j\pi \sin \theta}, \dots, e^{-j\pi(K-1) \sin \theta}]^T, \quad (5.3)$$

β_{ij} : Complex amplitude with Rayleigh distributed magnitude of j -th scattered sub-path

θ_i : Nominal DOA for i -th source

$\tilde{\theta}_{ij}$: DOA deviation of j -th sub-path of Gaussian random variable $\sim \mathcal{N}(0, \sigma_{\tilde{\theta}_i}^2)$

N_i : Number of sub-paths for i -th source

The superscript T denotes the transpose operator. $\Delta\theta_i$ is AS of $2\sigma_i$, where σ_i is the standard deviation of $\tilde{\theta}_{ij}$. This model neglects the time delays between the sub-paths, and $\tilde{\theta}_{ij}$ and β_{ij} have identically independent distribution (i.i.d) for the indices i and j . The observation period is assumed to be sufficiently short for the coherence time; hence, the channel is quasi-stationary in a burst frame duration [40].

5.4 Integrated System Functions

5.4.1 Estimation of Number of Sources

Based on Eigenvalue Decomposition

Since L is typically unknown, the MUSIC algorithm usually requires an estimate of the number of sources L as *priori*. We have some well-known criteria that determines the rank of the data vector \mathbf{x} from the estimated eigenvalues of the data matrix. These criteria, termed AIC (An Information Criterion) [46] and MDL (Minimum Description Length) [45] are given by

$$\text{AIC}(L) = -2N(K - L) \cdot \ln \delta(L) + K(2K - L) \cdot 2 \quad (5.4)$$

$$\text{MDL}(L) = -2N(K - L) \cdot \ln \delta(L) + K(2K - L) \cdot \ln N \quad (5.5)$$

respectively, where L , K , N , and λ denote the rank of the signal subspace (number of signals), number of elements, number of snapshots, and eigenvalues, respectively. The statistic quantity is given by

$$\ln \delta(L) = \frac{1}{K - L} \ln \left(\prod_{i=L+1}^K \lambda_i \right) - \ln \left(\frac{1}{K - L} \prod_{i=L+1}^K \lambda_i \right). \quad (5.6)$$

Based on the above criteria, we can estimate the number of signals as K to minimize $\delta(K)$.

There exists another simple criterion based on a heuristic approach that introduces the threshold levels to separate the signal and noise eigenvalues. The two threshold levels, λ_t from the maximum value and λ_b from the minimum value, are given as

$$\begin{cases} \Omega_t = \frac{\lambda_{\max}}{\lambda_t} \\ \Omega_b = \frac{\lambda_b}{\lambda_{\min}} \end{cases}, \quad (5.7)$$

respectively. The threshold levels should be applied to the provided situation.

Based on Power Spectrum

A number of signals can be estimated with the angular power spectrum, which is computed by a conventional beamformer [47]. In this approach, the threshold level in a power spectrum is also necessary. This approach is frequently used to effectively determine the number of clusters in multipath environments [48].

5.4.2 DOA Estimation

The fast DOA estimator termed UMP, implemented on FPGA [49], employs spectral unitary MUSIC algorithm and performs all computation processes with a fixed-point arithmetic. This arithmetic typically has a 16-bit finite word-length for low complexity and low power consumption that is superior to those of general-purpose processors. The resulting gate resources used in the target FPGA and the computation time required to process single burst frame defined

Table 5.1: Gate resouces and computation time.

	Used LEs (Equiv. Gates)	Computation Time (μs)
4-Element with SS	12,007 (280,760)	30.59
4-Element	12,995 (303,860)	57.11
8-Element	29,472 (689,130)	373.99

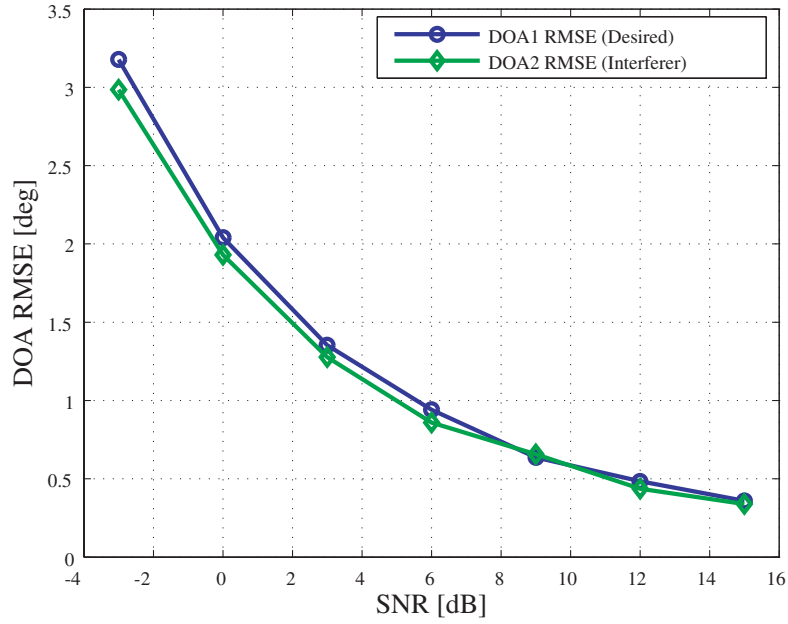


Fig. 5.5: DOA estimation in noise channel with UMP where two sources impinge at 4-element antenna array from 30° and -10° (planar wave assumption).

in Fig.5.3 are provided in Tab.5.1¹. Fig.5.5 shows DOA estimation examples of two incident signals with identical power in 4-element UMP, where the source locations are 30° and -10° . Each SNR used 2,000 burst frames. The detailed performance of the UMP has been discussed in Chapter 3. In fixed-point system, the arithmetic with fixed word-length usually lead to low dynamic range. In UMP, the estimation performance is also limited. The dynamic range of estimation performance depends on the word-length of the arithmetic processor in fixed point system. In addition, MUSIC DOA estimation performance with finite number of samples is limited by the SNR. The dynamic range was assessed by the success rates in the presence of multiple waves with difference powers which is defined as the rates satisfying the condition of

$$\boldsymbol{\vartheta} = |\boldsymbol{\theta}_{\text{estimated}} - \boldsymbol{\theta}_{\text{true}}| < \sqrt{L}, \quad (5.8)$$

¹The implementation results may not be optimum; however, it is important to note that better computation performance can be realized by enhancing parallelism and using a more efficient pipeline scheme.

where L is the number of waves. Figure 5.6 shows the success rates versus the power ratio between them assuming that two waves arrive at 8-element antenna array from 0 and 35° and sampled by a 12-bit ADC². When SNR is 10 dB as shown in Fig.5.6(a), the success rates are limited under SNR. Fig.5.6(b) shows the success rates in the SNR of 100 dB, where the noise contribution does not appear in the input signal sampled by 12-bit ADC. It is clarified that the performance degradation in the fixed point system, hence the word-length requirement should be examined depending on the applications.

5.4.3 User Identification

The simplest identification method is identifying the strongest of the received signals as the desired signal and the others as the interferers. This identification method is effective only if it is applied to relatively simple propagation environments. In the presence of a large number of multipaths comprising both the desired signal and interference components, the desired signal may not always be the strongest one. Further, it is certain that the strongest signal should be suppressed. [66] proposed an identification technique for all detected signals using pre-beamforming in practical environments. However, the pre-beamforming involves large computational tasks. On the other hand, the desired signal can be determined using a higher layer of the system control of periodic transmission with a relatively long unique word sequence and its correlation detection [55]. However, user identification is not included in the scope of this paper; we have assumed that the user signal is already known.

5.4.4 DOA Tracking

In a typical multipath propagation channel, the signal level becomes a random variable and the DOA is spread by local scatterers in the vicinity of the mobile terminals. Therefore, the beamforming with an instantaneous DOA estimation result based on the planar wave assumption leads to performance degradation. In small AS environments, such as an urban cellular base station, the statistical estimation by a tracker can be usefully introduced as

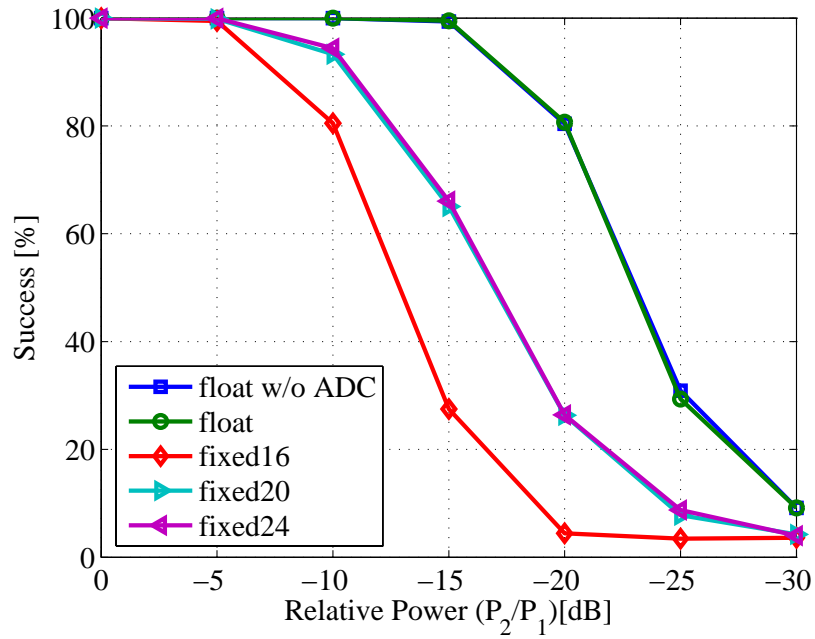
$$\tilde{\theta}_i(n) = \beta\tilde{\theta}_i(n-1) + (1-\beta)\theta_i(n), \quad (5.9)$$

where θ_i and $\tilde{\theta}_i$ are the instantaneous and tracked DOA, respectively. β is a forgetting factor (0.825 herein). Eq.(5.9) makes the estimation variation small, thus enabling the nominal DOAs to be tracked. Figures 5.7 and 5.8 show the estimation standard deviation of the DOA estimation with the 4-element UMP in a fading channel (AS is 3 degrees). In this simulation, 2000 burst frames were used, as shown in Fig.5.3, and it was shown that an averaging effect can be obtained by using the tracker. The averaging effect of tracker has been clearly illustrated in Fig.5.9.

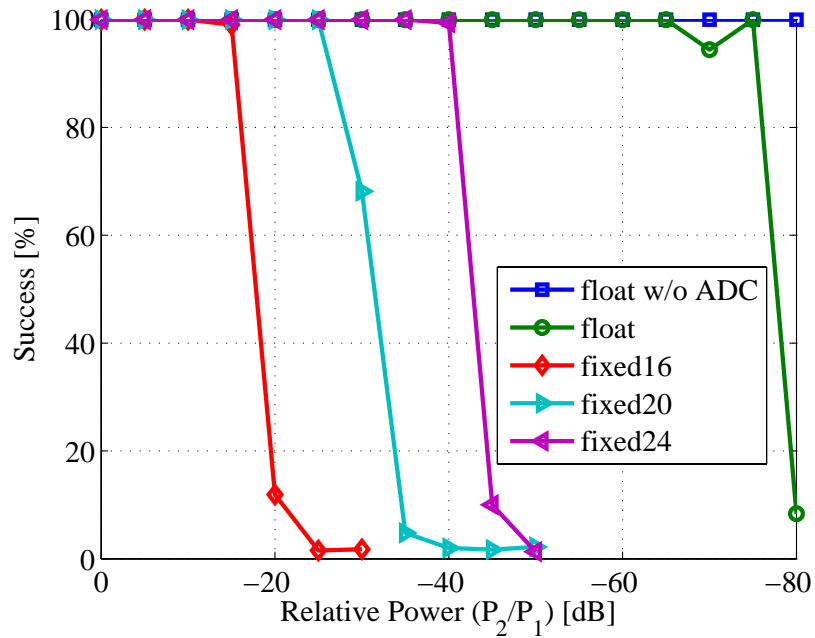
5.4.5 Beamforming

In this study, NDC-BF is applied, as discussed in Chapter 4. The in-beam interferers among estimated and classified signals are rejected by optional null-steering operation.

²The dynamic range of ADC is about 72 dB.



(a) SNR = 10 dB.



(b) SNR = 100 dB.

Fig. 5.6: Dynamic range of UMP (8-element antenna array from $s_1 = 0$ and $s_2 = 35^\circ$).

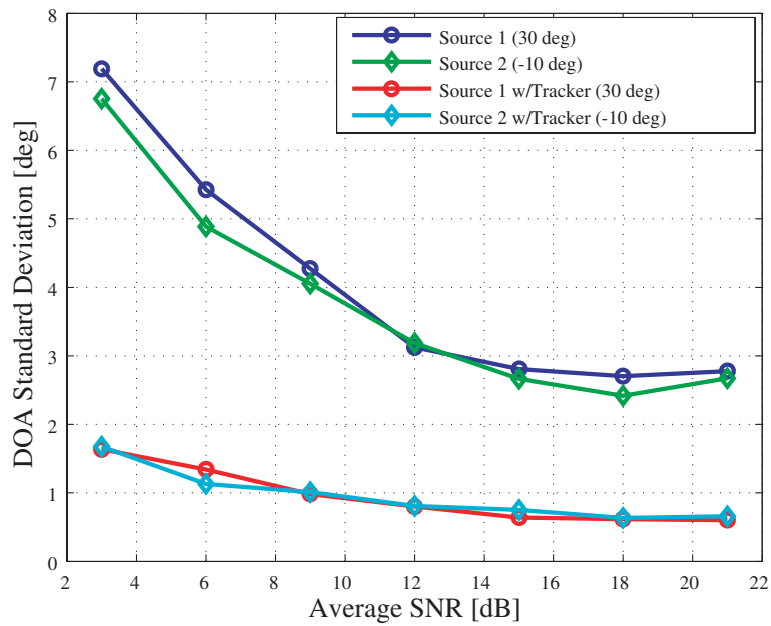


Fig. 5.7: Estimation standard deviations of instantaneous and tracked DOAs in Rayleigh fading channel with small angle spread ($AS=3^\circ$, source locations are 30 and -10°).

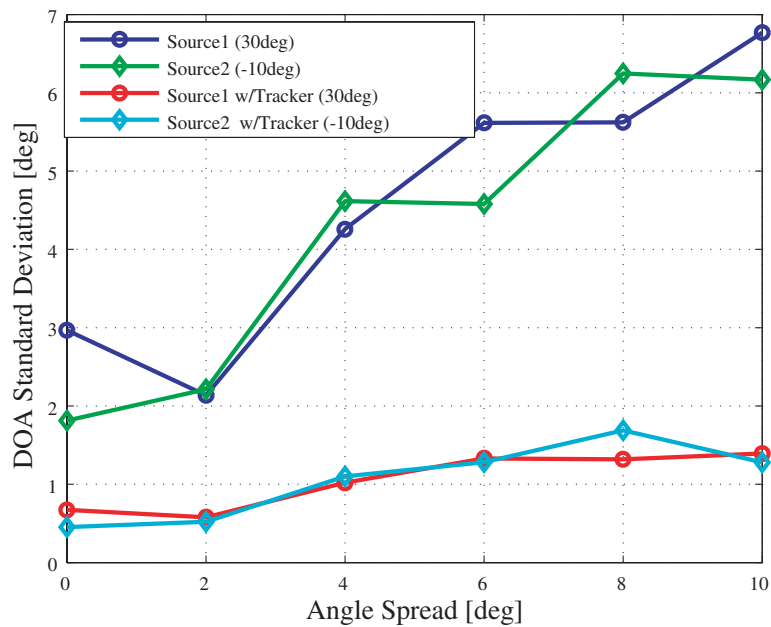
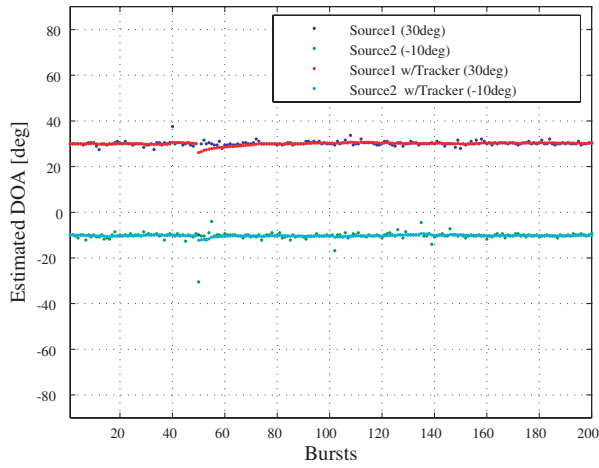
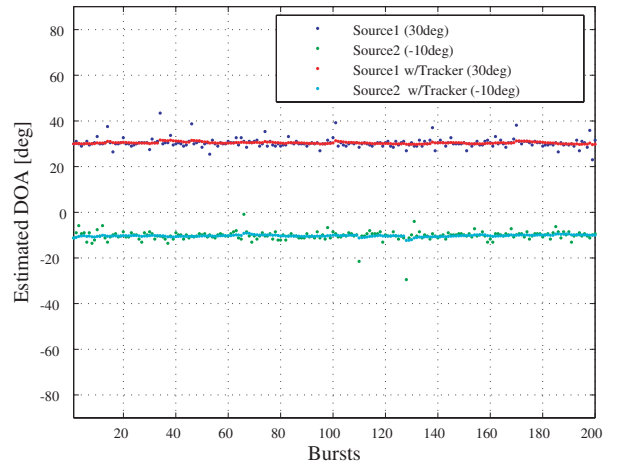


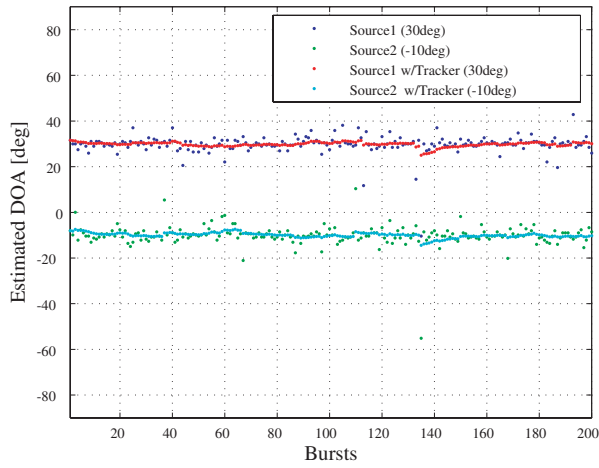
Fig. 5.8: Estimation standard deviations of instantaneous and tracked DOAs in Rayleigh fading channel with small angle spread ($SNR=13dB$, source locations are 30 and -10°).



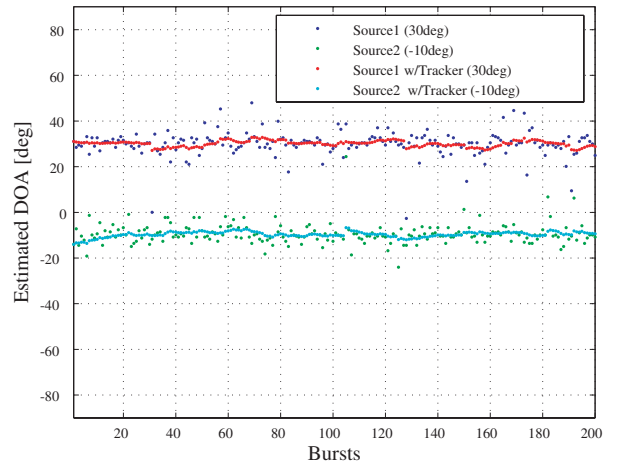
(a) $AS=0^\circ$



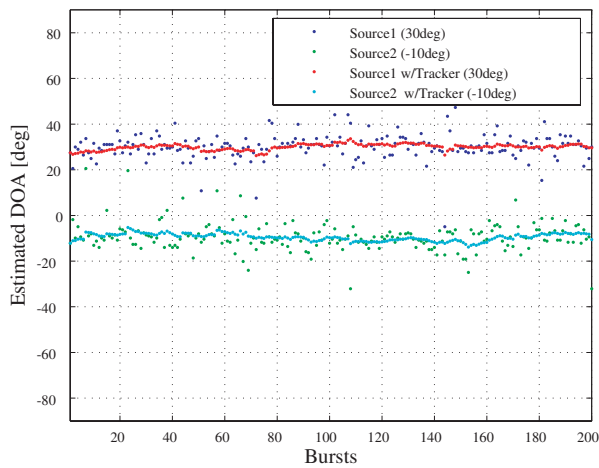
(b) $AS=2^\circ$



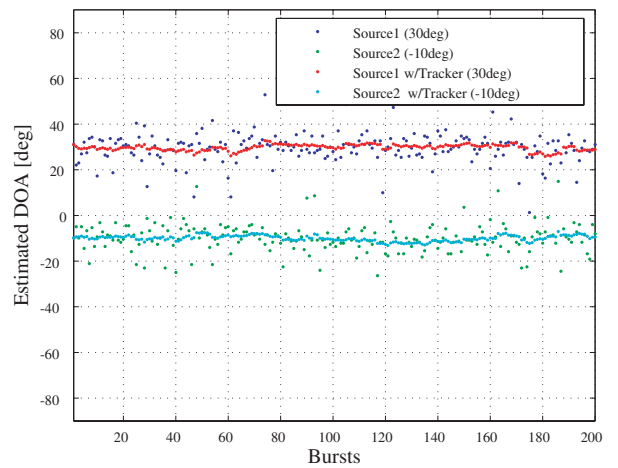
(c) $AS=4^\circ$



(d) $AS=6^\circ$



(d) $AS=8^\circ$



(e) $AS=10^\circ$

Fig. 5.9: Instantaneous DOA estimation results and tracked DOAs in Rayleigh fading channel with small angle spread (Source locations are 30 and -10°).

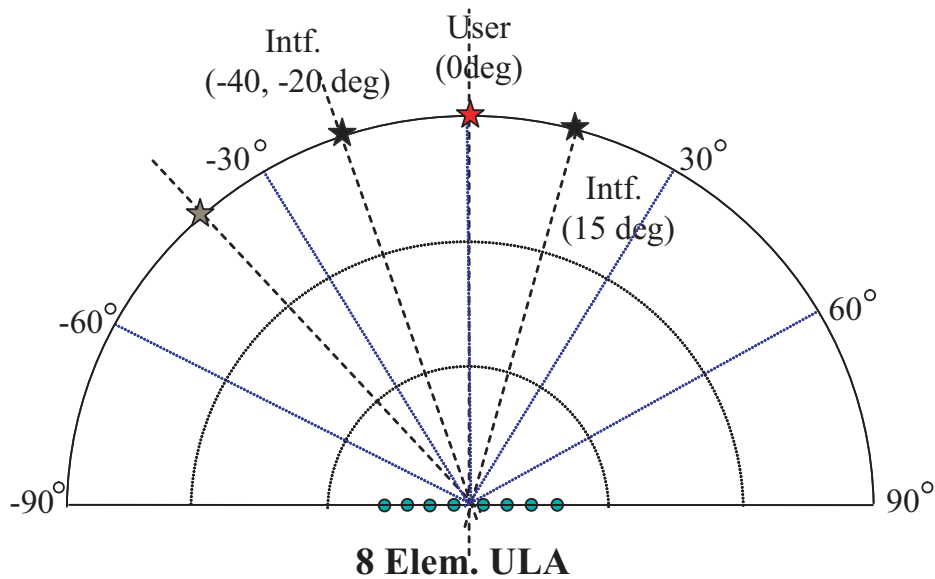


Fig. 5.10: Evaluation Model; LOS environment in noise channel.

5.5 Experimental Evaluations

This section evaluates the performance of the integrated system through experiments for certain cases.

5.5.1 Evaluation Model

The BER performance for urban cellular uplink channel was discussed in Chapter 4. However, in this section, the BER performance was analyzed experimentally. It was also assumed that four waves, including a single user and three interferers (two of them being in-beam interferers), arrived at the half-wavelength equi-spaced 8-element antenna array. The DOA estimation is carried out with a fixed-point UMP. Figure 5.10 is a schematic of the evaluation model in LOS environment with planar wave assumption without fading. The detailed parameters are also given in Tab.5.2. The performance of conventional (U-BF), low-sidelobe DC-BF, and ZF was computed for comparison with the proposed system. The typical beam patterns of various beamformers in this evaluation model are illustrated in Fig.5.11.

5.5.2 Measurement Setup

The measurement setup in a radio anechoic chamber is shown in Fig.5.12. The prototype processor in the developed testbed system includes the UMP DOA estimator and NDC beamformer processors. Further, it controls all measurement instruments for transceiver. The transmitting signals at an IF band of 10 MHz are generated by the digital-to-analog conversion and up-converted to RF band of 5 GHz. At the receiver, an 8-element ULA of sleeve antennas equi-spaced by $\lambda/2$ was employed. The received signals are downconverted to an IF band of 40 MHz and digitized by ADCs at 32 MHz using the undersampling technique. The

Table 5.2: Evaluation parameters.

Antennas	8-Element Sleeve ULA ($\lambda/2$)	
DOA Estimator	16-bit Fixed Point-UMP w/o Spatial Smoothing	
Beamformers	U-BF, DC-BF with SLR=40dB, NDC-BF with SLR=40dB, ZF	
Transmitting Signal	$\pi/4$ -DQPSK	
Burst Frame Length	136 Symbols (272 bits)	
Signal Sources	User	0°
	Interferers	$-20, 15^\circ$ (In-Beam), -40° (Out-of-Beam) Average INR @ single antenna of each signal is 9 dB (fixed)
Channels	LOS (AWGN)	
Trials	100	

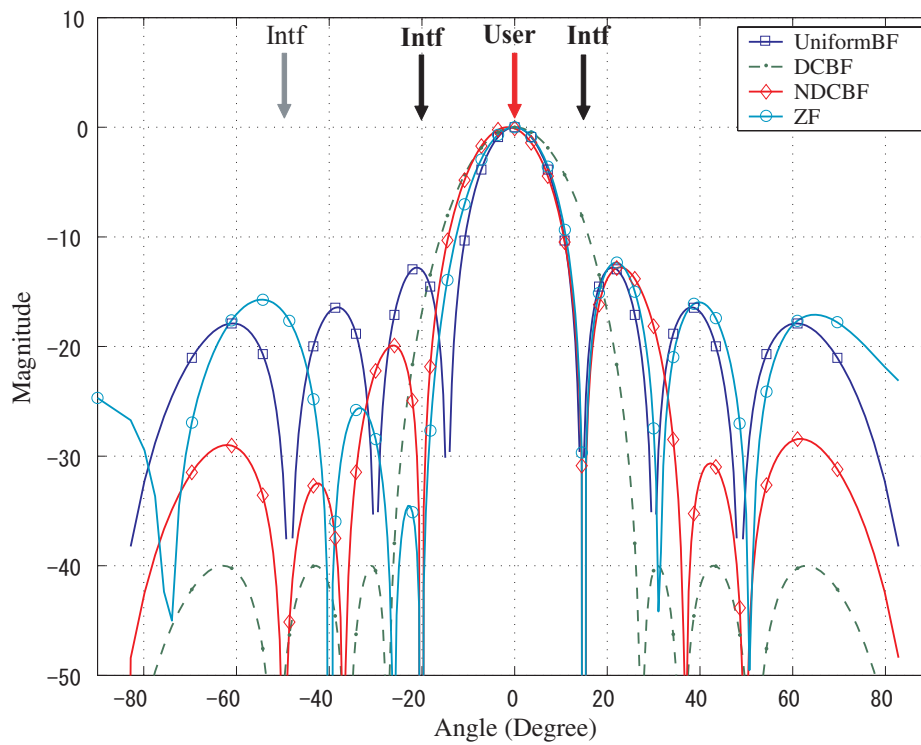


Fig. 5.11: Typical Beampatterns

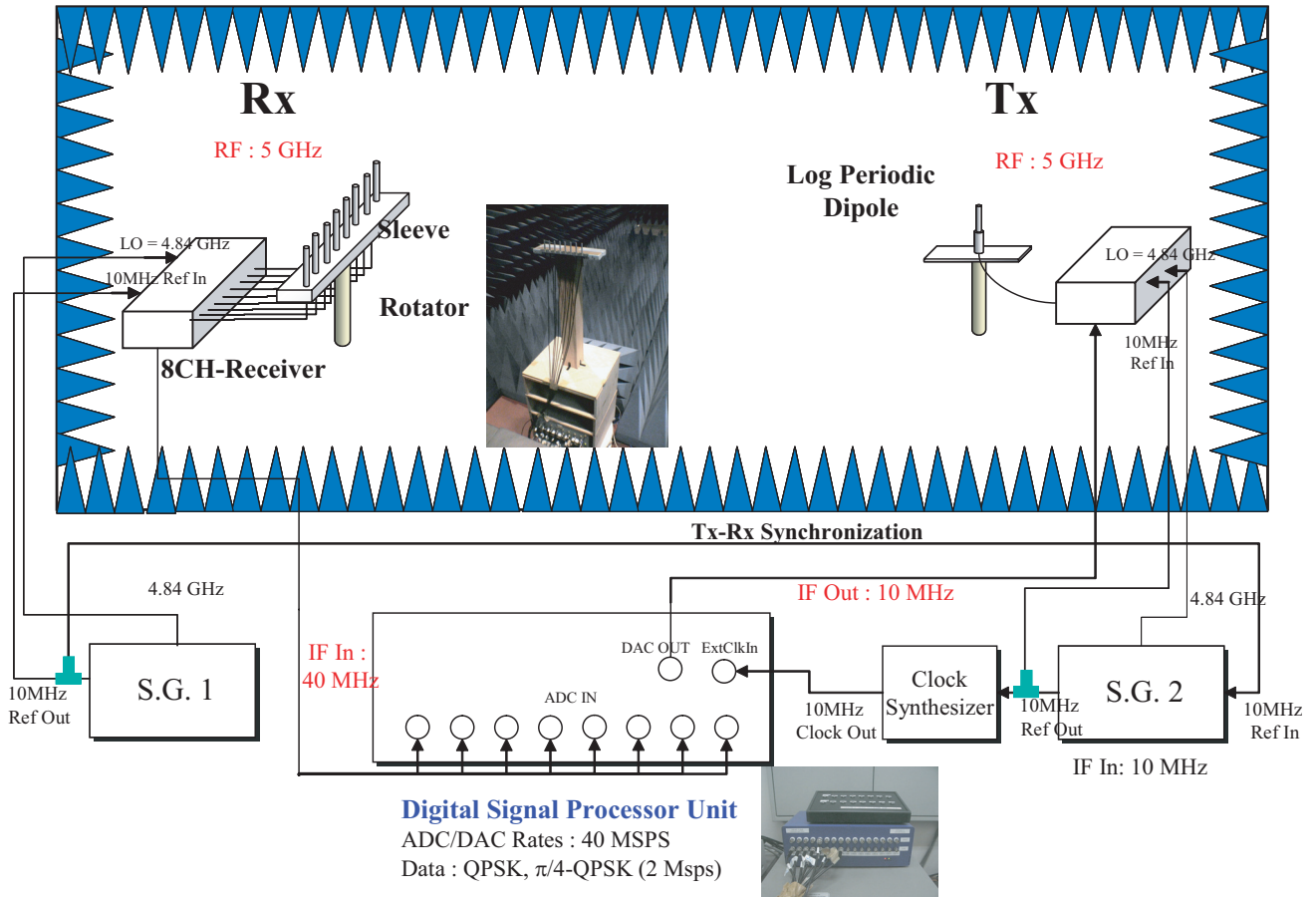


Fig. 5.12: Experimental Setup (Radio anechoic chamber)

symbol rates and modulation are 2 Msps (mega symbol per second) and $\pi/4$ -QPSK, respectively. Undersampling provides the frequency downconversion of the received signals from 40 MHz to 8 MHz; hence, the ADC's oversampling rates for symbol rates and carrier frequency are 16 ($32/2$) and 4 ($32/8$) times, respectively. The received signals are again downconverted into complex baseband signals during digital downconversion processing.

In this measurement setup, the carrier frequency was perfectly synchronized by direct connection between the local oscillators of the receiver and the transmitter via cable. Further, the operating clock of the prototype processor was also synchronized by a clock synthesizer, as shown in Fig.5.12. Thus, coherent detection can be performed.

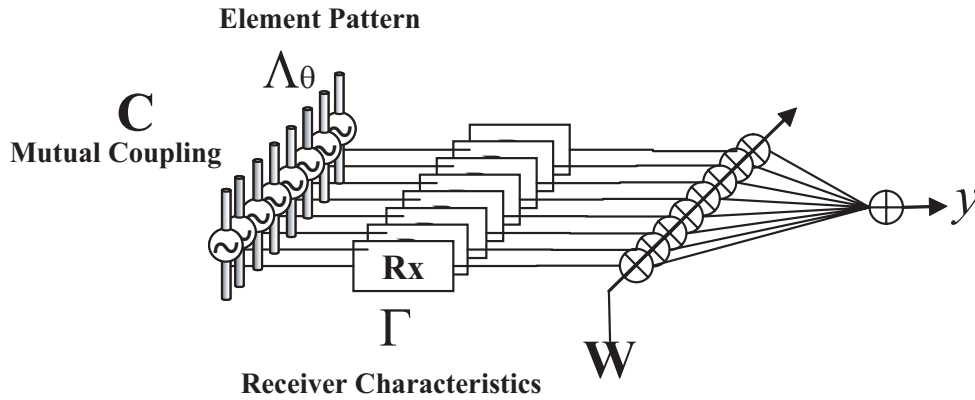


Fig. 5.13: Array antenna receiver in the presence of mutual coupling and initial receiver characteristics.

5.5.3 Antenna Array Calibration

In this study, each antenna in an antenna array system has been assumed to have an ideal omni-directional property. However, in general, the actual response of the antenna array significantly deviates from the assumed ideal model due to electromagnetic coupling among the antenna elements that are typically spaced closely by $\lambda/2$. In particular, in a spatial reference based system³ such as this study, a practical antenna response should be taken into careful consideration. Subspace based DOA estimators, such as MUSIC, require precise knowledge of the antenna array response from a standard source located in any direction. The collection of antenna array responses for all possible directions is termed as the array manifold. The performance of the subspace based system strongly depends on the accuracy of this array manifold [56]. However, in general, the measurement of an array manifold is generally a time-consuming task. There exist many studies of the mutual coupling effect in antenna arrays and a number of array calibration methods have been proposed [56–60]. The issue of array calibration is out of the scope of this work; hence, the mutual coupling effect in this system is only briefly discussed. In practice, the array calibration is performed using the compensation technique proposed in [59].

Formulation

Assuming that a signal $s_i(t)$ located at θ_i arrives at the K -element antenna array associated with mutual coupling \mathbf{C} , initial receiver characteristics $\mathbf{\Gamma}$, and element pattern $\mathbf{\Lambda}$, as shown in Fig.5.13, then the response of the array can be described by

$$\mathbf{x}_{\theta_i} = \mathbf{C}\mathbf{\Gamma}\mathbf{\Lambda}_{\theta_i}\mathbf{v}(\theta_i)s_i(t) + \mathbf{n}(t), \quad (5.10)$$

³It is also termed as angle domain system or DOA-based system.

where $n(t)$ is AWGN and \mathbf{C} , $\mathbf{\Gamma}$, and $\mathbf{\Lambda}$ are

$$\mathbf{C} = \begin{pmatrix} c_{11} & c_{12} & \cdots & c_{1K} \\ c_{21} & c_{22} & \cdots & c_{2K} \\ \vdots & \vdots & \ddots & \vdots \\ c_{K1} & c_{K2} & \cdots & c_{KK} \end{pmatrix}, \quad (5.11)$$

$$\mathbf{\Gamma} = \begin{pmatrix} \Gamma_1 & 0 & \cdots & 0 \\ 0 & \Gamma_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \Gamma_K \end{pmatrix}, \quad (5.12)$$

$$\mathbf{\Lambda} = \begin{pmatrix} \Lambda_1(\theta_i) & 0 & \cdots & 0 \\ 0 & \Lambda_2(\theta_i) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \Lambda_K(\theta_i) \end{pmatrix}, \quad (5.13)$$

respectively. For simplicity, the element pattern of each antenna is assumed to be omnidirectional; \mathbf{C} and $\mathbf{\Gamma}$ are replaced by the total error matrix \mathbf{G} by

$$\mathbf{x}_{\theta_i} = \mathbf{G}\mathbf{v}(\theta_i)s_i(t) + \mathbf{n}(t) \quad (5.14)$$

It is clear that the calibrated data vector can be obtained by multiplying the inversion of the total error matrix to the received data vector as

$$\begin{aligned} \tilde{\mathbf{x}}_{\theta_i} &= \mathbf{G}^{-1}\mathbf{x}_{\theta_i} \\ &= \mathbf{v}(\theta_i)s_i(t) + \mathbf{G}^{-1}\mathbf{n}(t), \end{aligned} \quad (5.15)$$

if the total error matrix can be estimated.

Total Error Matrix Estimation

The total error matrix is estimated by using the technique proposed in [59]. This technique exploits the orthogonality of the signal and noise subspace. The error matrix can be estimated with a smaller number of measured data than the array manifold technique. The received data from the i -th known source located at θ_i can be written as Eq.(5.14). The correlation matrix can be obtained by

$$\mathbf{R}_{\theta_i} = E[\mathbf{x}_{\theta_i}\mathbf{x}_{\theta_i}^H] = \sum_{j=1}^N \lambda_j^{(i)} \mathbf{e}_j^{(i)} \mathbf{e}_j^{(i)H}, \quad (5.16)$$

where λ_j and \mathbf{e}_j are the j -th eigenvalue and eigenvector, respectively. The following relation can be achieved using the orthogonality of signal and noise subspace, as

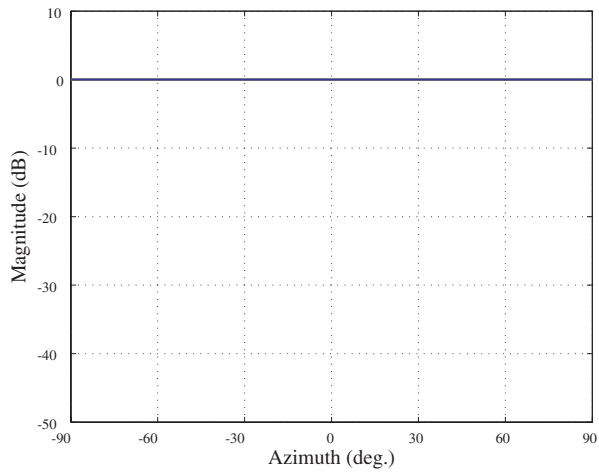
$$\mathbf{e}_j^{(i)H} \cdot \mathbf{G}\mathbf{v}(\theta_i) = 0, \quad j = 2, \dots, K \quad (5.17)$$

If the noise eigenvectors obtained by received data from a single known source are \mathbf{e}_j ($j = 2, \dots, K$), $K - 1$ equations can be achieved as

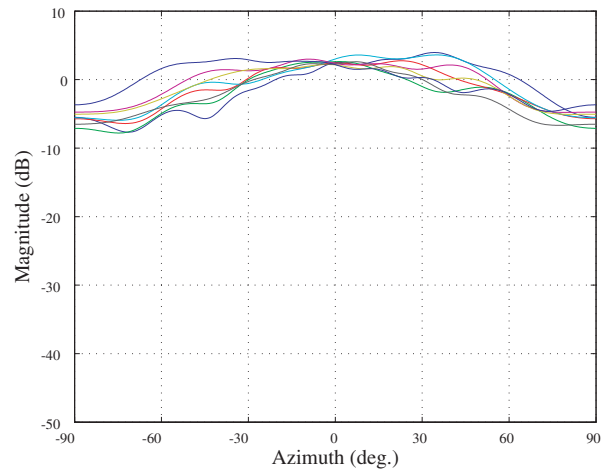
$$\mathbf{e}_j^{(i)H} \cdot \mathbf{G}\mathbf{v}(\theta_i) = [e_{j,1}^{(i)*}, e_{j,2}^{(i)*}, \dots, e_{j,K}^{(i)*}] \times \begin{bmatrix} g_{11}v_{i,1} + g_{12}v_{i,2} + \dots + g_{1K}v_{i,K} \\ g_{21}v_{i,1} + g_{22}v_{i,2} + \dots + g_{2K}v_{i,K} \\ \vdots \\ g_{K1}v_{i,1} + g_{K2}v_{i,2} + \dots + g_{KK}v_{i,K} \end{bmatrix} = 0, \quad (5.18)$$

where the number of unknown parameters is K^2 . For example, if $K = 8$ implies $K^2 = 64$ unknown parameters are given. Hence, a minimum of 10 independent data sets from known sources are required. Fig.5.14 shows the mutual coupling effect on the element patterns, where (a) and (c) represent an ideal case without mutual coupling while (b) and (d) represent a practical case with an estimated error matrix including mutual coupling and receiver characteristics. A sufficient number of independent data sets were collected to increase the estimation accuracy with known sources at specific locations (71 sets measuring at every 2° between -70° and 70°).

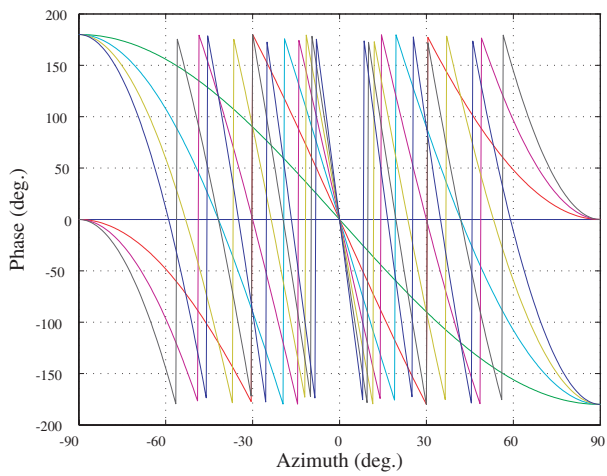
Fig.5.15 shows the improvement of DOA estimation accuracy with array calibration. The measurement conditions are that SNR is sufficiently high, above 30 dB, and the number of snapshots was 1,000 samples. It can be observed from the results that the array calibration with an estimated total error matrix effectively eliminates the error factor caused by mutual coupling and receiver characteristics. The harmful effect of mutual coupling appears with greater severity in the null-steering of adaptive beamformers.



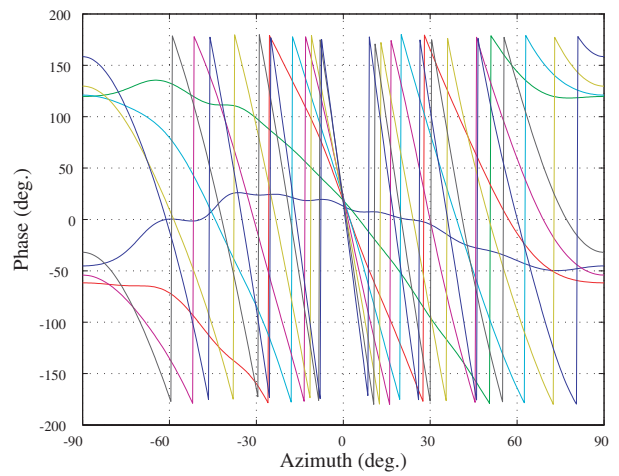
(a) Amplitude characteristics (ideal antenna array)



(b) Measured amplitude characteristics



(c) Amplitude characteristics (ideal antenna array)



(d) Measured amplitude characteristics

Fig. 5.14: Mutual coupling effect on element pattern of each antenna (8-element uniform linear array).

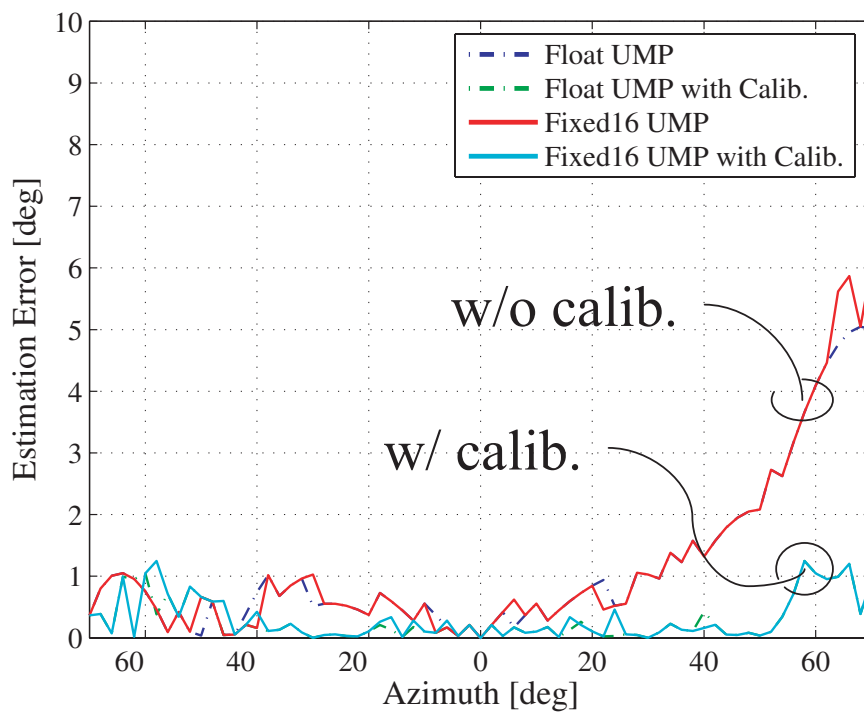


Fig. 5.15: Improvement of DOA estimation accuracy in 8-element UMP with array calibration.

5.5.4 Measurement in Anechoic Chamber

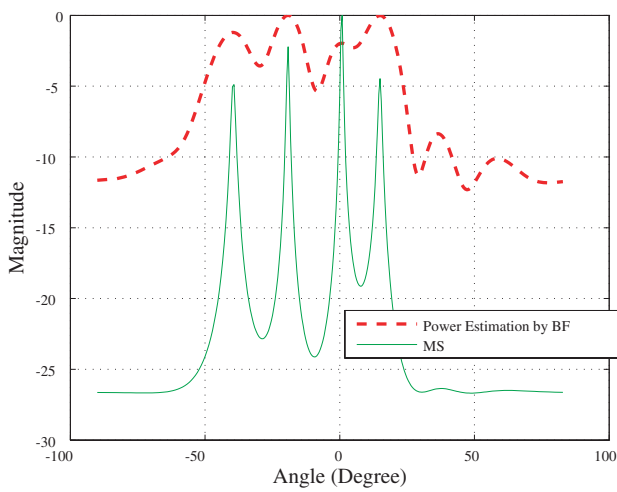
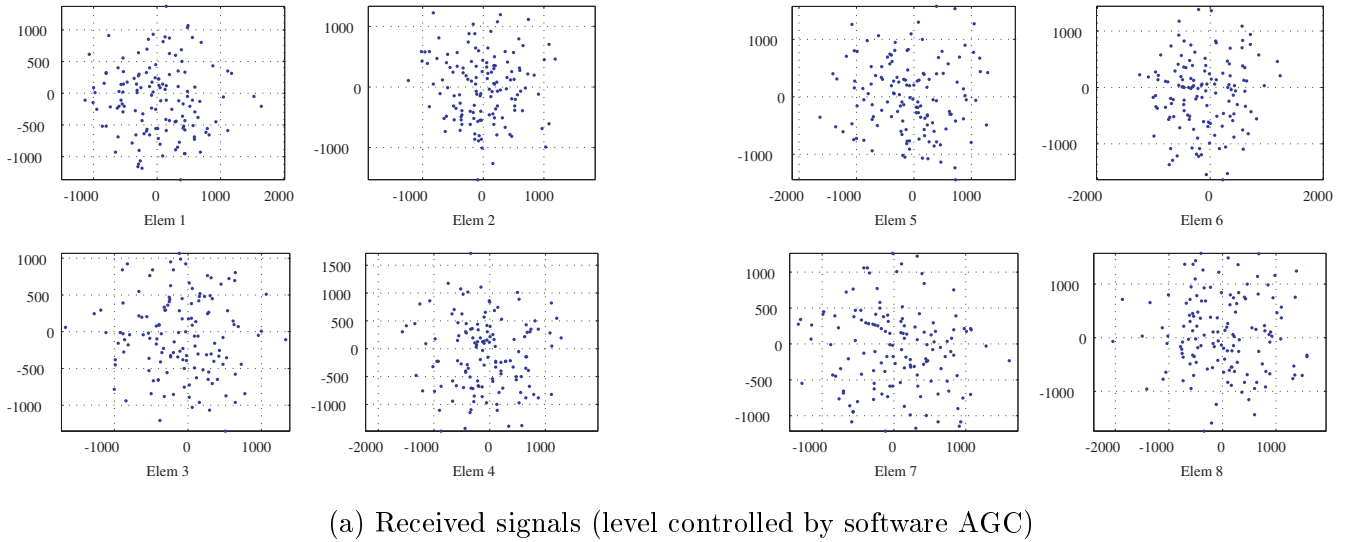
The BER (bit-error-rate) criterion is experimentally evaluated in order to verify the integrated system performance. The evaluation model is described in Tab. 5.2. In this study, the BER performance for two cases was measured. One case is when the actual DOAs are already known. This is not a practical case; however, the performance of the beamformer can be ideally evaluated regardless of the DOA estimation errors. The second case is when the DOAs are estimated by a developed UMP. It was assumed that the number of sources is already to be 4-one is the desired signal and the others are the interferers with INR (Interferer to Noise Ratio) of 9 dB. It is known that the DOA estimation performance will be significantly degraded when the number of sources is over- or under-estimated. The data vectors were obtained by combining each data vector with a single source, and the SNR was converted for the combined version of the data vector (see Appendix B).

The DOA estimation results by UMP, depending on the power of the desired signal, are shown in Fig.5.17. The UMP performs the DOA estimation with a fixed-point arithmetic, as described in Chapter 3; therefore, the dynamic range is usually low⁴. In this study, the allowable power difference for a normal estimation is approximately 15 dB without noise. Hence, the DOA estimation performance was degraded with a low SNR, as shown in Fig.5.17.

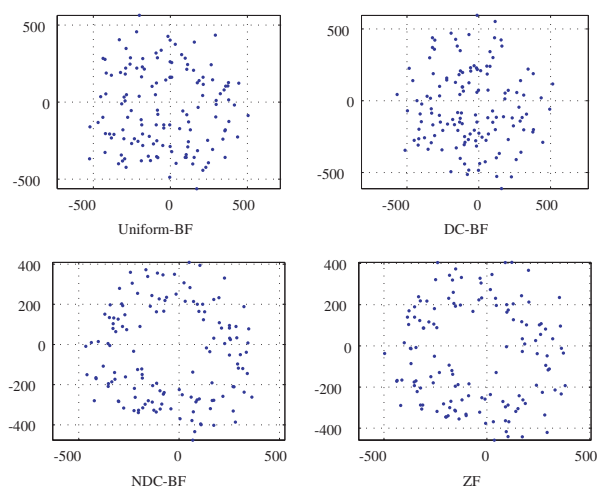
The mutual coupling and receiver characteristics usually have harmful effects on the DOA estimation and beamforming performance. The effects on ZF and NDC beamformers, in the presence of mutual coupling and receiver characteristics of a practical system, are illustrated in Fig.5.18. It is clarified that the pattern nulls do not have sufficient depth and are deviated from the desired locations. The shallow nulls result in the reception of unintentional interference power; hence, the quality of the desired signal will be typically degraded. Figure 5.16 provides an example of beamforming processing, where the SNR and INR were 6 dB and 9 dB, respectively. Further, Fig.5.19 shows the BER performance in various cases-in cases where the true DOAs were previously known, as in (a), (c), and (e) and those cases where the DOAs were estimated by UMP, as in (b), (d), and (f). It can be seen that the mutual coupling compensation provides improved performance close to the ideal antenna system as shown in Fig.5.19(e) and (f). It can also be seen that the DOA estimation errors lead to an increase in BER under the condition of low SNR, as shown in Fig.5.19(b), (d), and (f).

In Tabs.5.3 and 5.4, the results of the true DOA and UMP cases have been separately summarized. The gains G_1 and G_2 implies the differences of the required E_b/N_o to achieve the given BER performance (herein, BER = 0.01). It is clear that the proposed NDC-BF has comparable performance to the ZF beamformer and is superior to the uniform beamformer by 4.0 dB in a practical case in Tab.5.4.

⁴Generally, a low dynamic performance is the most critical problem in fixed-point systems.

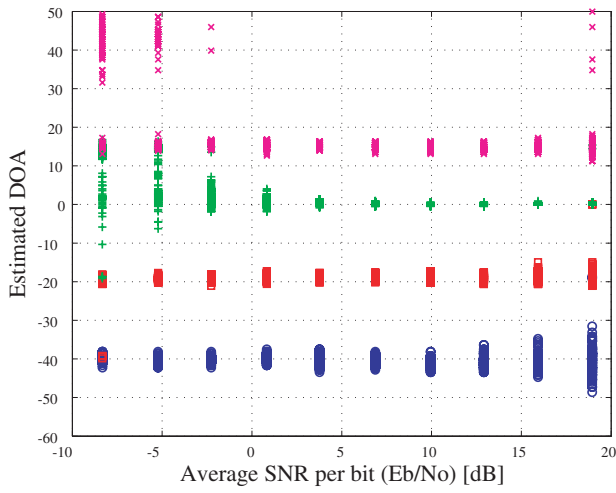


(b) DOA and relative power estimation

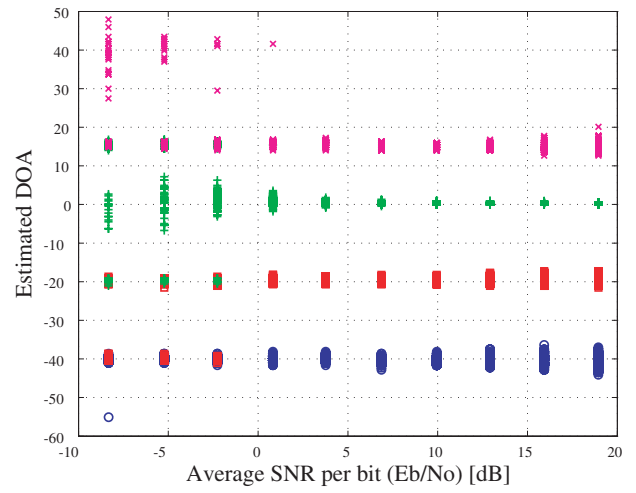


(c) Constellation after beamforming,
Error bits : 29(UBF), 71(DC), 16(NDC), 18(ZF)

Fig. 5.16: DOA estimation and beamforming example (SNR=6dB, INR=9dB).

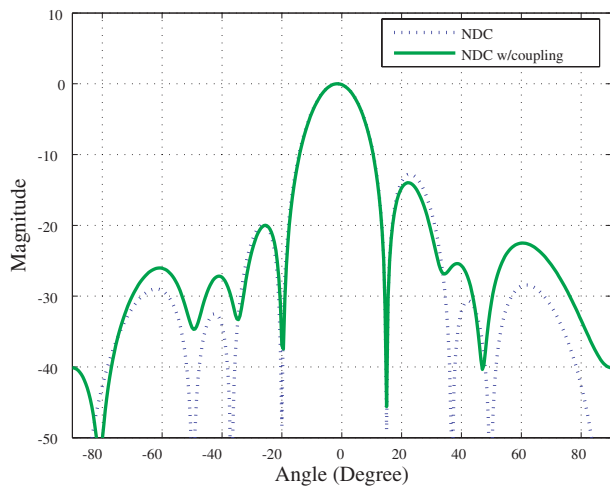


(a) without calibration

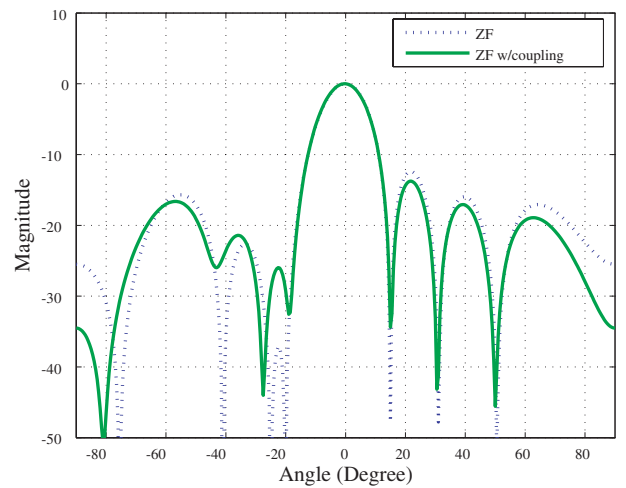


(b) with calibration

Fig. 5.17: DOA estimation results by UMP (true DOAs are -40 , -20 , 0 and 15° , 100 trials for a given desired signal's power (SNR), and the number of sources was set by 4).

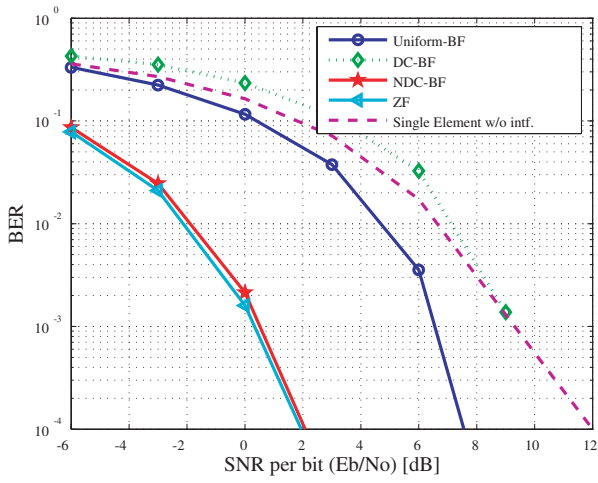


(a) Zero-forcing (ZF) beamformer.

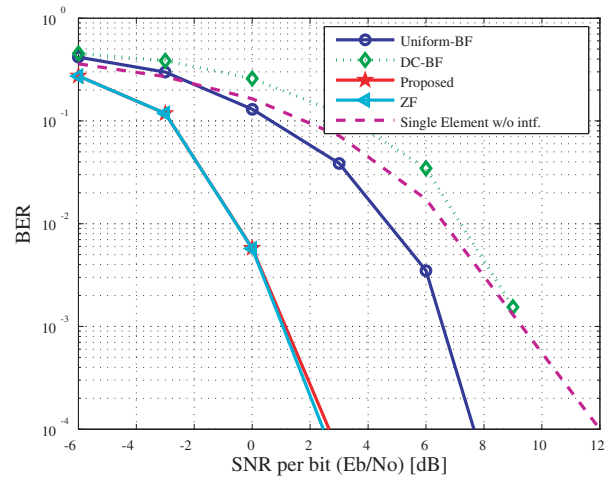


(b) Null-steering Dolph-Chebyshev (NDC) beamformer.

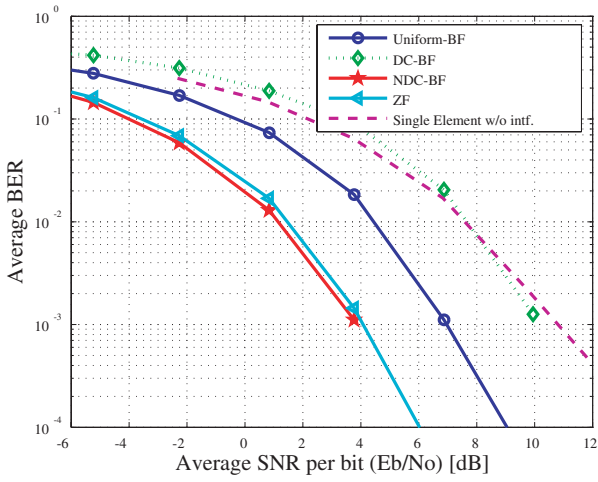
Fig. 5.18: Mutual coupling effect on beamforming.



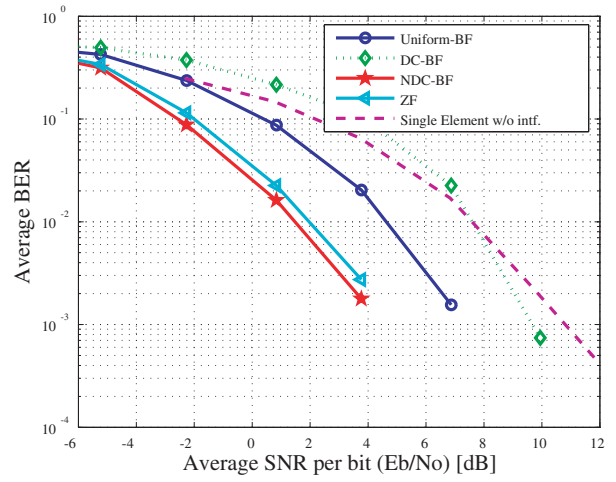
(a) Simulation (true DOAs)



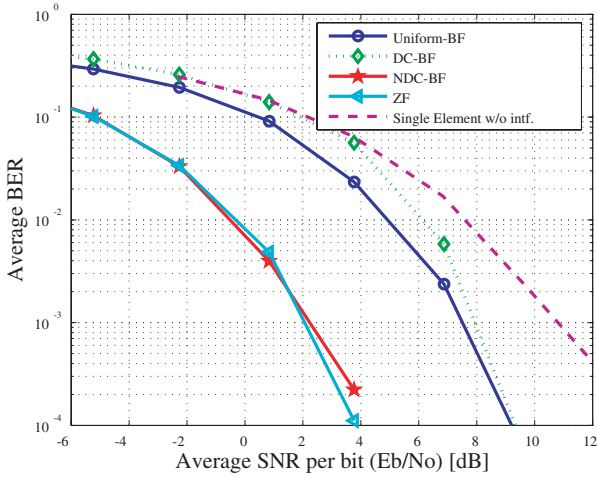
(b) Simulation (estimated by UMP)



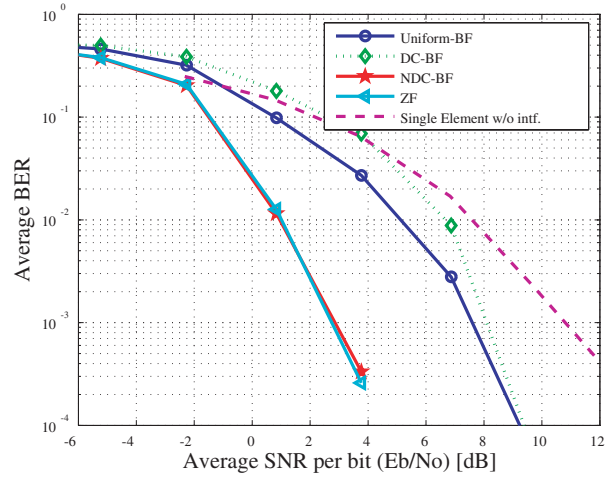
(c) Measurement (true DOAs)



(d) Measurement (estimated by UMP)



(e) Measurement with calibration (true DOAs)



(f) Measurement with calibration (estimated by UMP)

Fig. 5.19: BER Performances.

Table 5.3: E_b/N_0 Gains at BER=0.01 (True DOA).

unit [dB]	Required E_b/N_0					Gains	
	Single Elem. w/o Intfs (①)	U-BF (②)	DC-BF	ZF	NDC-BF (③)	G_1 (①-③)	G_2 (②-③)
Simulation	6.8	4.7	7.2	-2.1	-2.0	8.8	6.7
Measurement	7.5	4.2	7.8	1.2	1.0	6.5	3.2
Measurement (with Calibration)	7.5	4.9	6.0	-0.2	-0.3	7.8	5.2

Table 5.4: E_b/N_0 Gains at BER=0.01 (by UMP).

unit [dB]	Required E_b/N_0					Gains	
	Single Elem. w/o Intfs (①)	U-BF (②)	DC-BF	ZF	NDC-BF (③)	G_1 (①-③)	G_2 (②-③)
Simulation	6.8	4.2	7.2	-0.8	-0.8	7.6	5.0
Measurement	7.5	4.4	7.4	2.0	1.4	6.1	3.0
Measurement (with Calibration)	7.5	5.0	6.6	1.0	1.0	6.5	4.0

5.6 Summary

This chapter presented the experimental evaluation results with an integrated system assuming an uplink smart antenna system that is useful for macro-cellular base stations. The DOA estimator and beamformer were integrated on the developed testbed system. The evaluation system configuration co-designed by using FPGAs and CPU was introduced. Further, each processing function was discussed according to the processing flow and the computer simulation results were presented. This chapter also presented the experimental results of the total performance evaluation in a radio anechoic chamber assuming a LOS AWGN channel. Further, the problems of the calibration of antenna array and analog receivers were discussed.

Chapter 6

Conclusion

This section will summarize and conclude this paper.

The primary focus of this paper has been on the FPGA implementation of a smart antenna system including a DOA estimator and beamformer. This paper aims at the implementation of general signal processing independent of specific communication systems and hardware platforms. The prototype system integrating signal processors on FPGAs was manufactured and the evaluation testbed was configured. The prototype system employs an 8-element antenna array for the 5 GHz band and an RF transceiver for each branch. This paper verified the functionality of the baseband smart antenna processor via hardware level simulations and laboratory experiments. Further, this paper tested the entire hardware system including RF, antenna arrays, and air interface at both transmitter and receiver configurations in a radio anechoic chamber.

Chapter 2 comprised a detailed description of the developed hardware platforms of the smart antenna transceiver system including its implementation. The hardware requirements in smart antenna technologies have also been discussed. The benefits of the FPGAs as an array signal processor were described as compared to general-purpose DSP processors. The prototype transceivers take into consideration of the reconfiguration of an IF circuit as well as the adaptive control of an antenna beampattern in a SDR concept. In order to achieve this, the prototype transceivers are architected by low-IF super heterodyne with undersampling at receivers/harmonic band generation scheme at transmitters. In this chapter, the sampling jitter effect, which determines the maximum IF input frequency, was quantified based on measurements.

In this study, we succeeded in implementing the fixed-point processor of fast DOA estimator with FPGAs, as mentioned in Chapter 3. It incorporates the unitary MUSIC algorithm termed “UMP (Unitary MUSIC Processor).” This Unitary MUSIC algorithm has a super resolution capability and is suitable for integration on logic circuit devices such as FPGAs. The techniques suitable for FPGAs, such as eigenvalue decomposition by Cyclic Jacobi processor based on CORDIC and spectrum computation by spatial DFT (Discrete Fourier Transform), can be utilized to optimize it for fixed point arithmetic.

Chapter 4 proposed a novel beamforming technique for a DOA-based smart antenna system. This system basically steers the mainlobe for the user with the Dolph-Chebyshev beam.

Moreover in order to avoid undesirable interference reception by broad mainlobe, an optional null-steering processing cancels the interferers within the mainlobe coverage with notch beams, which are pre-computed and stored in the ROM. This is based on a cascade structure with Dolph-Chebyshev low-sidelobe and simple notch beampatterns to cancel the in-beam interferer; however, the weight vector can be obtained by simple convolution operations of the pre-computed Dolph-Chebyshev beam and the optional canceling beam. Hence, it has an extremely low complexity with a simple weighting operation that is suitable for implementation on high-speed logic devices, such as FPGAs. This paper has discussed the performance improvement and limitation of the proposed beamformer. Further, the BER performance in some cases was assessed through computer simulations.

Chapter 5 described the evaluation of the integrated system performance through a practical experiment. The effects caused by real hardware imperfection were discussed and array calibration issues were dealt with in this chapter. This chapter presented the evaluation results with an integrated system experimentally assuming uplink smart antenna system useful for macro-cellular base stations. The DOA estimator and beamformer were integrated on the developed testbed system. The evaluation system configuration co-designed by using FPGAs and CPU was introduced. Each processing function was discussed according to the processing flow and the computer simulation results were presented. The experimental results of total performance evaluation in a radio anechoic chamber assuming LOS AWGN channel were also presented. Further, the problems regarding the calibration of the antenna array and analog receivers were discussed.

Appendix A

FB Spatial Smoothing with Unitary Transformation

The real-valued correlation matrix is obtained with the unitary transformed forward only estimate \mathbf{R}_f as

$$\begin{aligned}\hat{\mathbf{R}} &= \text{Re} \{ \mathbf{Q}^H \mathbf{R}_f \mathbf{Q} \} \\ &= \frac{1}{2} (\mathbf{Q}^H \mathbf{R}_f \mathbf{Q} + (\mathbf{Q}^*)^H \mathbf{R}_f^* \mathbf{Q}^*) \\ &= \frac{1}{2} (\mathbf{Q}^H \mathbf{R}_f \mathbf{Q} + \mathbf{Q}^H \mathbf{J} \mathbf{R}_f^* \mathbf{J} \mathbf{Q})\end{aligned}\tag{A.1}$$

where the unitary transformation matrix \mathbf{Q} is column conjugate symmetric if

$$\mathbf{J} \mathbf{Q}^* = \mathbf{Q},\tag{A.2}$$

where \mathbf{Q} can be chosen as

$$\mathbf{Q} = \frac{1}{\sqrt{2}} \begin{pmatrix} \mathbf{I} & j\mathbf{I} \\ \mathbf{II} & -j\mathbf{II} \end{pmatrix}\tag{A.3}$$

or

$$\mathbf{Q} = \frac{1}{\sqrt{2}} \begin{pmatrix} \mathbf{I} & \mathbf{0} & j\mathbf{I} \\ \mathbf{0}^T & \sqrt{2} & -j\mathbf{0}^T \\ \mathbf{II} & \mathbf{0} & -j\mathbf{II} \end{pmatrix},\tag{A.4}$$

with an even and odd number of array elements, respectively, where the vector $\mathbf{0} = [0, 0, \dots, 0]^T$, and \mathbf{I} and \mathbf{II} are the identity matrix and column flipped identity matrix in the left-right direction, respectively [33, 35, 36].

Moreover Eq. (A.2) can be rewritten as

$$\begin{aligned}\hat{\mathbf{R}} &= \frac{1}{2} \mathbf{Q}^H (\mathbf{R}_f + \mathbf{J} \mathbf{R}_f^* \mathbf{J}) \mathbf{Q} \\ &= \frac{1}{2} \mathbf{Q}^H \mathbf{R}_{fb} \mathbf{Q},\end{aligned}\tag{A.5}$$

therefore we can achieve forward-and-backward (FB) spatial smoothing by the unitary transformation of forward-only correlation matrix.

Appendix B

SNR Conversion Relation

The received data vector only for i -th source is

$$\tilde{\mathbf{x}}_i = \mathbf{v}_i s_i(t) + \mathbf{n}(t), \quad (\text{B.1})$$

where additive noise $\mathbf{n}(t)$ is assumed to be spatially white as $E[\mathbf{n}(t)\mathbf{n}^H(t)] = \sigma_n^2 \mathbf{I}$. The SNR (signal-to-noise-ratio) is obtained by

$$S_i \text{NR} = \frac{P_i}{\sigma^2}. \quad (\text{B.2})$$

Using the linear combination of the collected data with single source the combined data vector for L sources is given by

$$\mathbf{x} = \sum_{i=0}^{L-1} \tilde{\mathbf{x}}_i = \mathbf{v}_0 s_0(t) + \sum_{i=1}^{L-1} \mathbf{v}_i s_i(t) + \sqrt{L} \cdot \mathbf{n}(t), \quad (\text{B.3})$$

where the noise amplitude is enhanced by \sqrt{L} times. Therefore $S_i \text{NR}$ for the i -th source can be obtained by

$$S_i \text{NR}^c = \frac{P_i}{L \cdot \sigma^2} \quad (\text{B.4})$$

where,

$$\begin{aligned} P_0 &= E[s_0^*(t) \cdot s_0(t)] = E[|s_0(t)|^2] \\ P_1 &= E[s_1^*(t) \cdot s_1(t)] = E[|s_1(t)|^2] \\ &\vdots \\ P_L &= E[s_L^*(t) \cdot s_L(t)] = E[|s_L(t)|^2] \end{aligned} \quad (\text{B.5})$$

Appendix C

Design Examples of Digital Signal Processing Unit

C.1 2-channel AD board

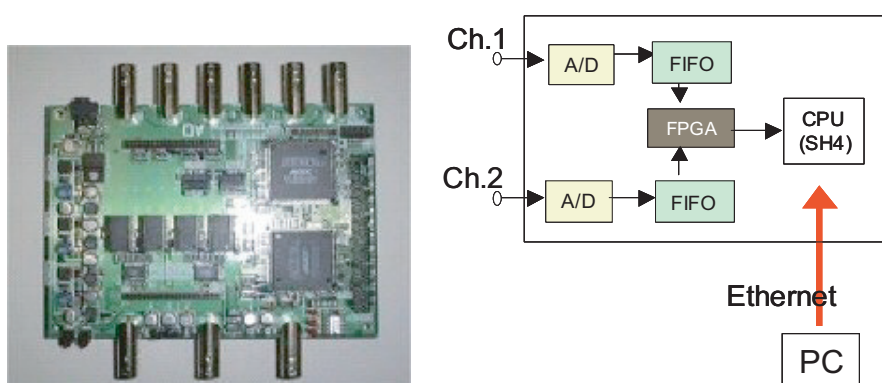


Fig. C.1: 2CH AD board.

ADC				
Part	Resolution	Sampling Rates	Power Consumption	Input BW
SPT 7938 (SPT)	12 bits	40 MSPS	170 mW	250MHz
Buffer Memory				
256 K Words / channel (FIFO)				
FPGAs				
ALTERA FLEX6K, ACEX1K100, FLEX10K200				

Table C.1: Specifications of 2CH AD board.

C.2 16-channel AD board

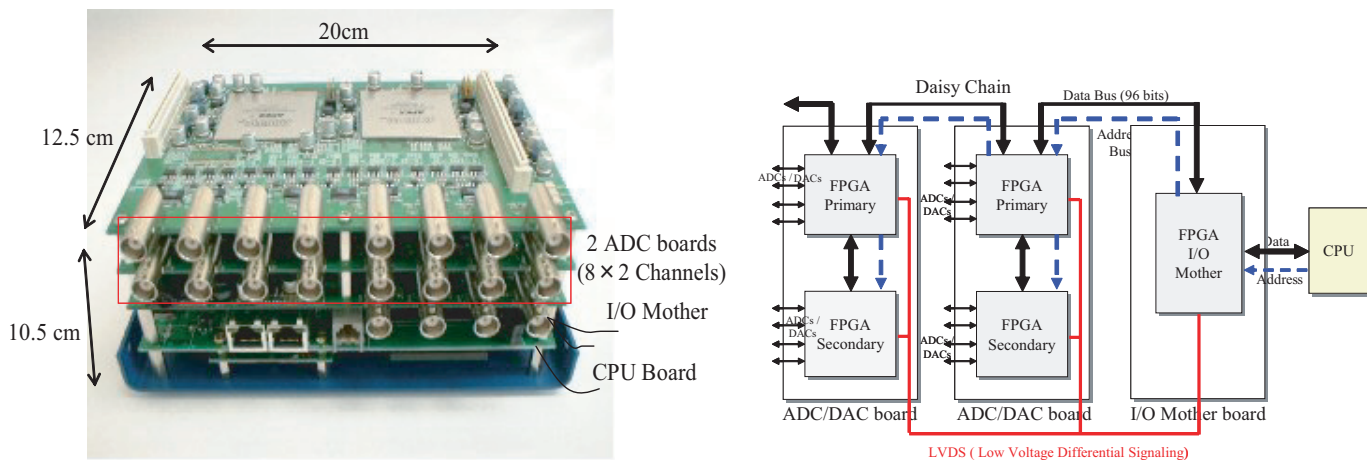


Fig. C.2: 16CH distributed architecture board.

ADC				
Part	Resolution	Sampling Rates	Power Consumption	Input BW
SPT 7938 (SPT)	12 bits	40 MSPS	170 mW	250MHz
DAC				
Part	Resolution	Sampling Rates	Power Consumption	
DAC 904 (Burrbrown)	14 bits	165 MSPS	170 mW	
FPGAs				
ALTERA APEX20KC (672pin, 0.6 Mega Gates, 311,296 memory bits)				

Table C.2: Specifications of 16CH distributed architecture board.

C.3 4-channel AD board

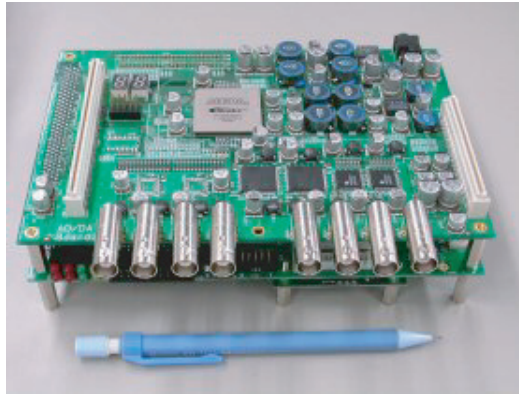


Fig. C.3: 4CH AD board.

ADC				
Part	Resolution	Sampling Rates	Power Consumption	Input BW
AD 9430 (Analog Device)	12 bits	200 MSPS	1.1 W	700MHz
ADS5422 (Burrbrown)	14 bits	62 MSPS	1.2 W	300MHz
DAC				
Part	Resolution	Sampling Rates	Power Consumption	
MAX 5192 (Maxim)	14 bits	260 MSPS	1.2 W	
FPGAs				
ALTERA STRATIX EP1S25 (780pin, 0.6 Mega Gates, 1,944,576 memory bits)				

Table C.3: Specifications of 4CH AD board.

C.4 16-channel AD/DA board

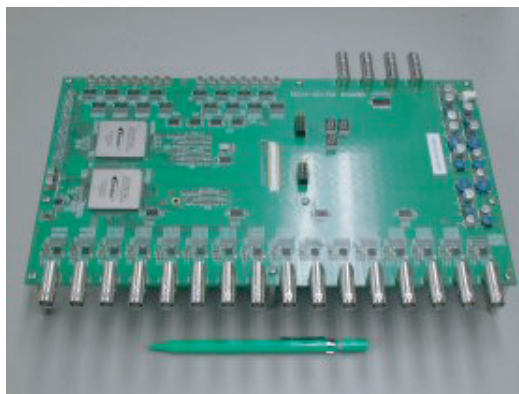


Fig. C.4: 16CH AD/DA board.

ADC				
Part	Resolution	Sampling Rates	Power Consumption	Input BW
AD 9245 (Analog Device)	14 bits	80 MSPS	366 mW	500MHz
DAC				
Part	Resolution	Sampling Rates	Power Consumption	
DAC 904 (Burrbrown)	14 bits	165 MSPS	170 mW	
Buffer Memory				
16 M Words / I,Q / channel (SDRAM DIMM module)				
FPGAs				
ALTERA STRATIX EP1S40(1020pin, 1 Mega Gates, 3,423,744 memory bits)				

Table C.4: Specifications of 16CH AD/DA board.

Bibliography

- [1] J. Proakis, *Digital communications*, New York; McGraw-Hill, 1989.
- [2] S. Haykin, *Adaptive filter theory*, Third Edition, Prentice Hall, 1996.
- [3] W. Jakes, Ed., *Microwave Mobile Communications*, New York: IEEE Press, 1974.
- [4] B. Widrow, P. Mantey, L. Griffiths and B. Goode, "Adaptive antenna systems," *IEEE Proceeding*, vol. 55, no. 12, pp. 2143-2159, Dec. 1967.
- [5] J. Liberti, Jr and T. Rappaport, *Smart antennas for wireless communications: IS-95 and third generation CDMA applications*, Prentice Hall PTR, 1999.
- [6] L. Godara, "Applications of antenna arrays to mobile communications part I : Performance improvement feasibility and system considerations," *Proceedings of the IEEE*, vol. 86, no. 7, pp. 1031–1061, July 1997.
- [7] L. Godara, "Applications of antenna arrays to mobile communications part II : Beamforming and direction-of-arrival considerations," *Proceedings of the IEEE*, vol. 85, no. 8, pp. 1195–1245, August 1997.
- [8] J. Winter, "Smart Antennas for Wireless Systems," *IEEE Personal Commun.*, vol. 5, no. 1, pp. 23–27, February 1998.
- [9] J. Litva and T. Lo, *Digital Beamforming in Wireless Communications*, Artech House Publishers, 1996.
- [10] H. Steyskal, "Digital Beamforming Antennas, An Introduction," *Microwave Journal*, Vol. 30, No. 1, pp. 107-124, January. 1987.
- [11] P. Lehne and M. Pettersen, "An Overview of Smart Antenna Technology for Mobile Communications Systems," *IEEE Communications Surveys*, Fourth Quarter, 1999, Vol. 2, No. 4, <http://www.comsoc.org/pubs/surveys>.
- [12] N. Kikuma, *Adaptive Signal Processing with Array Antenna*, Science and Technology Publishing Company, Inc., 1999 (in Japanese).
- [13] N. Kikuma and M. Fujimoto, "Adaptive antennas," *IEICE Trans. Commun.*, vol. E86-B, no. 3, pp. 968–979, March 2003.

- [14] H. Arai and K. Cho, "Cellular and PHS base station antenna systems," *IEICE Trans. Commun.*, vol. E86-B, no. 3, pp. 980–992, March 2003.
- [15] Y. Ogawa and T. Ohgane, "Advances in Adaptive Antenna Technologies in Japan," *IEICE Trans. Commun.*, Vol. E84-B, no. 7, pp. 1704–1712, July 2001.
- [16] S. Anderson, M. Millnert, M. Viberg and B. Wahlberg, "An adaptive array for mobile communication systems," *IEEE Trans. Veh. Technol.*, vol. 40, no. 1, pp. 230–236, Feb. 1991.
- [17] R. Kohno, "Spatial and temporal communication theory using adaptive antenna array," *IEEE Personal Communications*, pp. 28–35, Feb. 1998.
- [18] A. Paulraj and B. Ng, "Space-time modems for wireless personal communications," *IEEE Personal Communications*, pp. 36–48, Feb. 1998.
- [19] H. Taoka, S. Tanaka, T. Ihara and M. Sawahashi, "Adaptive Antenna Array Transmit Diversity in FDD Forward Link for W-CDMA and Broadband Packet Wireless Access," *IEEE Wireless Communications*, vol. 9, pp. 34–41, Apr. 2002.
- [20] S. Tanaka, T. Ihara, M. Sawahashi, "Optimum Weight Generation Method for Adaptive Antenna Array Transmit Diversity in W-CDMA Forward Link," *IEICE Trans. Commun.*, vol. E84-A, no. 12, pp. 3035–3044, Dec. 2001.
- [21] M. Mikami and T. Fujii, "An Antenna Weight Control Method of Downlink for Adaptive Array Antennas at Base Station in DS-CDMA Cellular System," *IEICE Trans. Commun.*, vol. J87-B, no. 9, pp. 1174–1184, Sept. 2004 (in Japanese).
- [22] P. Howells, "Intermediate frequency sidelobe canceller," *U.S. Patent 3202990*, Aug. 1966.
- [23] R. Ertel, P. Cardieri, K. Sowerby, T. Rappaport and J. Reed "Overview of spatial channel models for antenna array communication systems," *IEEE Personal Communications Magazine*, pp. 10–22, Feb. 1998.
- [24] S. Ichitsubo, K. Tsunekawa, Y. Ebibe "Multipath Propagation Model of Spatio-Temporal Dispersion Observed at Base Station in Urban Areas," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 6, pp. 1204–1210, Aug. 2002.
- [25] S. Ichitsubo, K. Tsunekawa, Y. Ebibe "Multipath Propagation Model of Spatio-Temporal Dispersion Observed at Base Station in Urban Areas," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 6, pp. 1204–1210, Aug. 2002
- [26] T. Ohtsu, N. Umeda and M. Minomo, "Special Articles on Fourth-Generation Wireless Access Technology: Toward Next-Generation Mobile Communications Systems, (1) The Fourth-Generation Mobile Communication Systems" *NTT DoCoMo Technical Journal*, vol. 11, no. 2, pp. 6–69, Jul. 2003 (in Japanese).

- [27] G. Foschini and M. Gans, "On Limits of Wireless Communications in a Fading Environment when Using Multiple Antennas", *Wireless Personal Communications*, vol. 6, pp.311–335, 1998.
- [28] G. Focschini, G. Golden, R. Valenzuela and P. Wolniansky, "Simplified Processing for High Spectral Efficiency Wireless Communication Employing Multi-Element Arrays", *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 11, pp. 1841–1852, Nov. 1999.
- [29] S. Alamouti, "A simple transmit diversity technique for wireless communications", *IEEE Journal on Selected Areas in Communications*, vol. 16, no. 8, pp. 1451–1458, Oct. 1998.
- [30] V. Tarokh, N. Seshadri and A. Calderbank, "Space-time codes for high data rate wireless communication : performance criterion and code construction", *IEEE Trans. Inform. Theory*, vol. 44, no. 2, pp. 744–765, March 1998.
- [31] R. Schmidt, "Multiple emitter location and signal parameter estimation," *IEEE Trans. Antennas and Propag.*, vol. 34, no. 3, pp. 276–280, March 1986.
- [32] R. Roy and T. Kailath, "ESPRIT - Estimation of signal parameters via rotational invariance techniques," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-37, pp. 984–995, 1989.
- [33] K. Huarng and C. Yeh, "A unitary transformation method for angle of arrival estimation," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 39, no. 4, pp. 975–977, Apr. 1991.
- [34] M. Pesavento, A. Gershman and M. Haardt, "On unitary root-MUSIC with a real-valued eigendecomposition: A theoretical and experimental performance study," *IEEE Trans. Signal Processing*, vol. 48, no. 5, pp. 1306–1314, May 2000.
- [35] M. Zoltowski, G. Kautz and S. Silverstein, "Beamspace root-MUSIC," *IEEE Trans. Signal Processing*, vol. 41, no. 1, pp. 344–364, Jan. 1993.
- [36] M. Haardt and J. Nossék, "Unitary ESPRIT: How to obtain increased estimation accuracy with a reduced computational burden," *IEEE Trans. Signal Processing*, vol. 43, no. 5, pp. 1232–1242, May 1995.
- [37] P. Stoica and A. Nehorai, "MUSIC, Maximum Likelihood, and Cramer-Rao Bound," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 37, no. 5, pp. 720–741, May 1989.
- [38] P. Stoica and A. Nehorai, "Performance Study of Conditional and Unconditional Direction-of-Arrival Estimation," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 38, no. 10, pp. 1783–1795, Oct. 1990.
- [39] P. Stoica and A. Nehorai, "MUSIC, Maximum Likelihood, and Cramer-Rao Bound: Further Results and Comparisons," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 38, no. 12, pp. 2140–2150, Dec 1990.

- [40] D. Astely and B. Ottersten, "The effects of local scattering on direction of arrival estimation with MUSIC," *IEEE Trans. Signal Processing*, vol. 47, no. 12, pp. 3220–3234, Dec. 1999.
- [41] D. Astely and B. Ottersten, "Modified array manifold for signal waveform estimation in wireless communications," in Proc. *30th Asilomar Conf. Signals, Syst., and Comput.*, pp. 738–741, Nov. 1996.
- [42] M. Bengtsson and B. Ottersten, "Signal waveform estimation from array data in angular spread environment," in Proc. *30th Asilomar Conf. Signals, Syst., and Comput.*, pp. 355–359, Nov. 1996.
- [43] J. Jeong, K. Sakaguchi, K. Araki and J. Takada, "Generalization of MUSIC using extended array mode vector for joint estimation of instantaneous DOA and angular spread," *IEICE Trans. Commun.*, vol. E84-B, no. 7, pp. 1781–1789, July 2001.
- [44] T. Shan, M. Wax and T. Kailath, "On Spatial Smoothing for Direction-of-Arrival Estimation of Coherent Sources," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 33, no. 4, pp. 806–811, Aug. 1985.
- [45] M. Wax and T. Kailath, "Detection of signals by information theoretic criteria," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 33, no. 2, pp. 387–392, Apr. 1985.
- [46] H. Akaike, "A new look at the statistical model identification," *IEEE Trans. Automatic Control*, vol. 19, no. 6, pp. 716–723, Dec. 1974.
- [47] E. Matsuzaki and H. Arai, "DOA and Number of the Waves Estimation under Multipath Environments using Beamformer Methods," in Proc. *IEICE society conference*, B-1-119, Sept. 2003.
- [48] S. Kikuchi, A. Sano, H. Tsuji and R. Miura, "A Novel Approach to Mobile-Terminal Positioning Using Single Array Antenna in Urban Environments," in Proc. *IEEE Vehicular Technology Conference (VTC)*, Orlando, FL, US, Oct. 2004.
- [49] M. Kim, K. Ichige and H. Arai, "Implementation of FPGA based Fast DOA Estimator using Unitary MUSIC algorithm," in Proc. *IEEE Vehicular Technology Conference (VTC)*, Orlando, FL, US, Oct. 2003.
- [50] B. Van Veen and K. Buckley, "A Versatile Approach to Spatial Filtering," *IEEE ASSP Magazine*, pp. 4-24, Apr. 1988.
- [51] C. Dolph, "A current distribution for broadside arrays which optimizes the relationship between beamwidth and sidelobe level," *Proc. IRE*, vol. 34, no. 6, pp. 335–348, 1946.
- [52] L. Griffiths and K. Buckley, "Quiescent Pattern Control in Linearly Constrained Adaptive Arrays," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-35, no. 7, pp. 917–926, Aug. 1987.

- [53] D. Asztely and B. Ottersten, "Modified array manifold for signal waveform estimation in wireless communications," in Proc. *30th Asilomar Conf. Signals, Syst., and Comput.*, pp 738-741, Nov. 1996.
- [54] K. Takao, M. Fujita and T. Nishi, "An adaptive antenna array under directional constraints," *IEEE Trans. Antenna and Propag.*, AP-24, 5, pp. 662-669, Sept. 1976.
- [55] T. Asai, S. Tomisato and T. Matsumoto, "Field test results for a beam and null simultaneous steering S/T-equalizer in broadband mobile communication environments," *IEICE Trans. Commun.*, vol. E84-B, no. 7, pp. 1760-1767, July 2001.
- [56] B. Friedlander and A. Weiss, "Direction Finding in the Presence of Mutual Coupling," *IEEE Trans. Antenna and Propag.*, vol. 39, No. 3, pp. 273-284, Mar. 1991.
- [57] K. Dandekar, H. Ling and G. Xu, "Experimental Study of Mutual Coupling Compensation in Smart Antenna Applications," *IEEE Trans. Wireless Commun.*, vol. 1, No. 3, pp. 480-487, Jul. 2002.
- [58] A. Wyglinski and S. Blostein, "On Uplink CDMA Cell Capacity: Mutual Coupling and Scattering Effects on Beamforming," *IEEE Trans. Veh. Technol.*, vol. 52, No. 2, pp. 289-304, Mar. 2003.
- [59] T. Arai, R. Hara, H. Yamada and Y. Yamaguchi, "On Calibration of Superresolution Array Using Known Sources," *IEICE Trans. Commun.*, vol. J85-B, no. 3, pp. 527-535, Sept. 2003 (in Japanese).
- [60] Y. Inoue and H. Arai, "Effect of Mutual Coupling and Manufacturing Error of Array for DOA Estimation of ESPRIT Algorithm," *IEICE Trans. Commun.*, vol. J86-B, no. 10, pp. 2145-2152, Oct. 2003 (in Japanese).
- [61] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," in Proc. *the 1998 ACM/SIGDA sixth international symposium on Field Programmable Gate Arrays*, pp. 192-200, Monterey, CA, Feb. 1998.
- [62] B. Fawcett and R. Iwanczuk, "Techniques and Tools for FPGA-based DSP design," in Proc. *International Conference on Signal Processing Application and Technology (ICSPAT)*, San Diego, CA, Sept. 1997.
- [63] R. Baines, "The DSP Bottleneck," *IEEE Communications Magazine*, pp. 46-54, May 1995.
- [64] *Implementing FIR filters in FLEX Devices*, ALTERA Applications Note 73, Feb. 1998
- [65] R. Miura, T. Tanaka, A. Horie and Y. Karasawa, "A DBF Self-Beam Steering Array Antenna for Mobile Satellite Applications Using Beam-Space Maximal-Ratio Combination," *IEEE Trans. Veh. Technology*, Vol. 48, No 3, May 1999.

- [66] A. Kuchar, M. Tangemann and E. Bonek, "A real-time DOA-Based smart antenna processor," *IEEE Trans. Veh. Technol.*, vol. 51, No. 6, pp. 1279–1293, Nov. 2002.
- [67] T. Horiuchi, "Applications of BSD for embedded use," *Interface*, Chapter 6, CQ publishing, pp. 101–110, Aug. 2002 (in Japanese).
- [68] M. Kim, H. Arai and M. Fukuta "Development of a Digital Prototype Board for Adaptive Array Antenna Receiver," *2001 IEICE Communication Society Conference*, B-1-151, The University of Electro-Communications, Chofu, Japan, Sep. 2001.
- [69] M. Kim, K. Ichige and H. Arai, "Adaptive array antenna experimental system based on FPGAs and its evaluation through implementation of MRC beamformer," *IEICE Technical Report*, AP2002-38, June 2002.
- [70] S. Muramatsu, M. Kim, K. Ichige, H. Arai, "A Prototype Transmitter Using FPGA and Adaptive Antenna Array for High-Speed Mobile Communication System," *IEICE Antenna Propagation Technical Report, Wireless Communication Workshop*, AP2003-14, YRP, Japan, Mar. 2003.
- [71] S. Muramatsu, *A Study of Designing Digital Part of Adaptive Array Antenna Transceiver and Receiver*, Master's thesis, Electrical and Computer Eng., Yokohama National University, January 2002 (in Japanese).
- [72] M. Kim, K. Ichige and H. Arai, "DOA-based Adaptive Array Antenna Testbed System," in Proc. *2003 IEEE AP-S Topical Conference on Wireless Communication Technology*, pp. 374-375, Honolulu, HI, US, Oct. 2003.
- [73] H. Arai and M. Kim, "Hardware Design of RF and Digital Units for Smart Antenna System," in Proc. *Asia Pacific Microwave Conference (APMC)*, Nov. 2003.
- [74] M. Kim, K. Ichige and H. Arai, "Implementation of FPGA based Fast Unitary MUSIC DOA Estimator," *IEICE Trans. Electron.*, Vol. E87-C, no. 9, pp. 1485–1494, Sept. 2004.
- [75] M. Kim, K. Ichige and H. Arai, "Real-time Smart Antenna System Incorporating FPGA-based Fast DOA Estimator," in Proc. *2004 IEEE Vehicular Technology Conference (VTC 2004 fall)*, Los Angeles, CA, US, Sept. 2004.
- [76] *Digital IF Subsampling Using the HI5702*, HSP45116 and HSP43220, Intersil Application Note, AN9509.2.
- [77] R. Cupo, G. Golden, C. Martin, K. Sherman, N. Sollenberger, J. Winter and P. Wolniansky, "A Four-Element Adaptive Antenna Array for IS-136 PCS Base Stations," in Proc. *1997 IEEE Vehicular Technology Conference (VTC 1997 spring)*, Phoenix, AZ, US, May, 1997.
- [78] R. Kohno, "Structures and theories of software antennas for software defined radio," *IEICE Trans. Commun.*, vol. E83-B, no. 6, pp. 1189–1199, June 2000.

- [79] Y. Karasawa, "The Software Antenna: A New Concept of Kaleidoscopic Antenna in Multimedia Radio and Mobile Computing Era," *IEICE Trans. Commun.*, Vol. E80-B, No. 8, pp.1214–1217, Aug. 1997.
- [80] J. Mitola, "The Software Radio Architecture," *IEEE Communications Magazine*, vol. 33, No. 5, pp. 26–38, May 1995.
- [81] M. Cummings and S. Haruyama, "FPGA in the software radio," *IEEE Communications Magazine*, vol. 37, no. 2, pp.108–112, Feb 1999.
- [82] A. Rudra, "FPGA-based applications for software radio," *RF Design (www.rfdesign.com)*, May 1, 2004, Web documents are available at http://rfdesign.com/mag/radio_fpgabased_applications_software/index.html.
- [83] R. Vaughan, N. Scott and D. White, "The theory of bandpass sampling," *IEEE Trans. on Signal Processing*, vol. 39, No. 9, pp. 1973–1984, Sept. 1991.
- [84] J. Wepman, "Analog-to-Digital Converters and Their Applications in Radio Receivers," *IEEE Communications Magazine*, pp. 39–45, May 1995.
- [85] R. Groshong and S. Ruscak, "Undersampling Techniques Simplify Digital Radio," *Electronic design*, vol. 39, No. 10, pp. 67–78, May 1991.
- [86] H. Kobayashi, K. Kobayashi, M. Morimura, Y. Onaya, Y. Takahashi, K. Enomoto and H. Kogure, "Sampling Jitter and Finite Aperture Time Effects in Wideband Data Acquisition Systems," *IEICE Trans. Fundamentals*, vol. E85-A, No. 2, pp. 335–346, Feb. 2002.
- [87] M. Shinagawa, Y. Akazawa and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-state Circuits*, vol. 25, no. 1, pp.220–224, Feb. 1990.
- [88] M. Nagahora, A. Yokoi, T. Naito, S. Ohira and K. Isawa, "Effect of clock jitters on bandpass sampling," in Proc. *IEICE Society Conference*, SB-10-4, Sept. 1999, in Japanese.
- [89] P. Kenington and L. Astier, "Power Consumption of A/D Converters for Software Radio Applications," *IEEE Trans. Veh. Technol.*, vol. 49, No. 2, pp. 643–650, Mar. 2000.
- [90] National Semiconductor application note 775, *Specifications and Architectures of Sample-and-Hold Amplifiers*, July 1992, Web documents are available at <http://www.national.com/an/AN/AN-775.pdf>.
- [91] *AD9430 Datasheet*, Analog Device, 2002. Web documents are available at <http://www.analog.com>.
- [92] Altera Technical Brief, *Jitter Comparison Analysis: APEX 20KE PLL vs. Virtex-E DLL*, Web documents are available at <http://www.altera.com/literature/tb/tb70.pdf>.
- [93] M. Drutarovsky, V. Fischer and R. Lukac, "True Random Number Generator in Altera ACEX Devices," in Proc. *the XVII Conference on Design of Circuits and Integrated Systems, DCIS2002*, pp. 587-592, Santander, Spain, Nov. 2002.

- [94] A. Kiyono, M. Kim, K. Ichige and H. Arai, "Jitter Effect on Digital Downconversion Receiver with Undersampling Scheme," in Proc. *The 2004 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS2004)*, Hiroshima, Japan, July 2004.
- [95] T. Fuji, M. Kim, K. Ichige and H. Arai, "Use of Alias Harmonic Components in D/A conversion for Generating High Frequency IF Signals," in Proc. *The 2004 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS2004)*, Hiroshima, Japan, July 2004.
- [96] G. Golub and C. Van Loan, *Matrix Computations*, The Johns Hopkins University Press, 1996.
- [97] W. Press, S. Teukolsky, W. Vetterling and B. Flannery, *Numerical Recipes in C, The Art of Scientific Computing*, Second Edition, Cambridge University Press, 1992.
- [98] J. Gotze, S. Paul and M. Sauer, "Efficient Jacobi-like Algorithm for Parallel Eigenvalue Computation," *IEEE Trans. Computer*, vol. 42, No. 9, pp. 1058–1065, Sep. 1993.
- [99] J. Muller, *Elementary Functions: Algorithms and Implementation*, Birkhäuser, 1997.
- [100] J. Volder, "The CORDIC trigonometric computing technique," *IRE Trans. Electronic Computing*, Vol. EC-8, 1959.
- [101] M. Kim, K. Ichige and H. Arai, "Design of Jacobi EVD processor based on CORDIC for DOA estimation with MUSIC algorithm," *IEICE Trans. Commun.*, vol. E85-B, no. 12, pp. 2648–2655, Dec 2002.
- [102] *APEX 20KC Programmable Logic Device Data Sheet*, Altera Corp., Web document is available at http://www.altera.co.jp/literature/ds/ds_apex20kc.pdf.
- [103] *Stratix Device Handbook*, Altera Corp., Web document is available at http://www.altera.com/literature/hb/stx/stratix_handbook.pdf.
- [104] *FFT MegaCore Function User's Guide*, Altera Corp., Web document is available at <http://www.altera.com/literature/ug/fftug.pdf>.

Publication list

Related Works

Journal Papers

1. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Design of Jacobi EVD processor based on CORDIC for DOA estimation with MUSIC algorithm," *IEICE Transactions on Communications*, Vol. E85-B, No.12, pp. 2648–2655, Dec. 2002.
2. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Implementation of FPGA based Fast Unitary MUSIC DOA Estimator," *IEICE Transactions on Electronics*, Vol. E87-C, No. 9, pp. 1485–1494, Sept. 2004.
3. Minseok Kim, Aiko Kiyono, Koichi Ichige and Hiroyuki Arai, "Jitter Effect on Digital Downconversion Receiver with Undersampling Scheme," *IEICE Transactions on Information and System* (Submitted).
4. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "DOA-based smart antenna implementation," (preparing)

Proceedings of International Conferences

5. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "FPGA-Based DSP Implementation of Simple MRC beamformer," *2001 Asia Pacific Microwave Conference (APMC 2001)*, pp.589–592, National Taiwan University, Taipei, Taiwan, Dec. 2001.
6. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Design of JACOBI EVD Processor Based on CORDIC for DOA Estimation with MUSIC Algorithm," *The 13th IEEE Symposium on Personal, Indoor and Mobile Radio Commun. (PIMRC2002)*, Vol. 1, pp. 120–124, Lisbon, Portugal, Sept. 2002.
7. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Implementation of FPGA based Fast DOA Estimator using Unitary MUSIC Algorithm," *2003 IEEE Vehicular Technology Conference (VTC 2003 fall)*, Vol. 1, pp. 213–217, Orlando, FL, US, Oct. 2003.
8. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "DOA-based Adaptive Array Antenna Testbed System," *2003 IEEE AP-S Topical Conference on Wireless Communication Technology*, pp. 374–375, Honolulu, HI, US, Oct. 2003.

9. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Real-time Smart Antenna System Incorporating FPGA-based Fast DOA Estimator," *2004 IEEE Vehicular Technology Conference (VTC 2004 fall)*, Los Angeles, CA, US, Sept. 2004.

IEICE Technical Reports (Domestic)

10. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "FPGA-Based DSP Implementation of Simple MRC Digital Beamforming Antenna," *IEICE Antenna Propagation Technical Report*, AP2001-49, Kitami Institute of Technology, Hokkaido, JAPAN, Jul. 2001.
11. Minseok Kim, Koichi Ichige, Hiroyuki Arai and Koichi Tsunekawa, "Adaptive Array Antenna Experimental System based on FPGAs and its evaluation through implementation of MRC beamformer," *IEICE Antenna Propagation Technical Report*, AP2002-38, Tokyo, JAPAN, June. 2002.
12. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Performance Evaluation of fast DOA Estimator and DOA-based Beamforming," *IEICE Antenna Propagation Technical Report*, AP2004-18, Iwate Univ., JAPAN, May 2004 (in Japanese).

Proceedings of IEICE General / Society Conferences (Domestic)

13. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Examination of FPGA Implementation on Eigenvalue Decomposition in MUSIC Method," *2001 IEICE General Conference*, B-1-45, Ritsumeikan Univ., Kyoto, JAPAN, Mar. 2001
14. Minseok Kim, Koichi Ichige, Hiroyuki Arai and Masahiro Fukuta, "Development of a Digital Prototype Board for Adaptive Array Antenna Receiver," *2001 IEICE Communication Society Conference*, B-1-151, The University of Electro-Communications, Chofu, JAPAN, Sep. 2001
15. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Design of EVD Computation Processor for MUSIC DOA Estimation by Using Cyclic Jacobi Method based on CORDIC," *2002 IEICE General Conference*, A-4-70, Waseda University, Tokyo, JAPAN, Mar. 2002
16. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Design of Fast DOA Estimator using Unitary MUSIC Algorithm based on FPGA," *2003 IEICE General Conference*, B-1-118, Tohoku University, Sendai, JAPAN, Mar. 2003
17. Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Performance Evaluation of FPGA-based Fast DOA Estimator," *2004 IEICE General Conference*, B-1-230, Tokyo Inst. of Tech., Tokyo, JAPAN, Mar. 2004

Other Conferences

18. Minseok Kim, Yuki Inoue, Kohei Mori and Hiroyuki Arai, "DOA Estimation using DBF Array Antenna and FPGA-based DSP Implementation," *2000 KEES General Conference*, B-1-230, Choongnam Univ., Taejeon, Korea, Sept. 2000

Joint Works

Journal Papers

19. Atsushi Nakajima, Minseok Kim, Hiroyuki Arai, "FPGA Implementation of MMSE Adaptive Array Antenna using RLS algorithm," *IEICE Transactions on Communications* (Japanese Edition) (submitted).

Proceedings of International Conferences

20. Kohei Mori, Yuki Inoue, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "DBF array antenna systems at 8.45 GHz," *International Symposium of IEEE Antenna and Propagation Society (APS2001)*, pp. 222–225, Boston, MA, US, June 2001.
21. Hiroyuki Arai and Minseok Kim, "Hardware Design of RF and Digital Units for Smart Antenna System," *2003 Asia Pacific Microwave Conference (APMC 2003)*, Seoul, Korea, Nov. 2003.
22. Tatsuo Fuji, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Use of Alias Harmonic Components in D/A conversion for Generating High Frequency IF Signals," *The 2004 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS2004)*, Hiroshima, Japan, Jul. 2004.
23. Aiko Kiyono, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Jitter Effect on Digital Downconversion Receiver with Undersampling Scheme," *The 2004 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS2004)*, Hiroshima, Japan, Jul. 2004.
24. Atsushi Nakajima, Minseok Kim and Hiroyuki Arai, "Performance Evaluation of MMSE Adaptive Array using FPGA," *2004 Korea-Japan AP/EMC/EMT Joint Conference (KJJC-AP/EMC/EMT'04)*, Seoul National University, Seoul, Korea, Nov. 2004.
25. Atsushi Nakajima, Minseok Kim and Hiroyuki Arai, "FPGA Implementation of MMSE Adaptive Array Antenna using RLS algorithm," *International Symposium of IEEE Antenna and Propagation Society (APS2005)*, June. 2005 (submitted).

IEICE Technical Reports (Domestic)

26. Shintaro Muramatsu, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "A Prototype Transmitter Using FPGA and Adaptive Antenna Array for High-Speed Mobile Communication System," *IEICE Antenna Propagation Technical Report, Wireless Communication Workshop*, AP2003-14, YRP, JAPAN, Mar. 2003.
27. Naoya Matsumoto, Minseok Kim, Koichi Ichige and Hiroyuki Arai "FPGA Implementation of MMSE Adaptive Array Antenna using RLS algorithm," *IEICE Antenna Propagation Technical Report*, AP2003-210, Kanazawa Univ., JAPAN, June 2003 (in Japanese).

Proceedings of IEICE General / Society Conferences (Domestic)

28. Shintaro Muramatsu, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "A Study of Implementation of the System for DOA Estimation by MUSIC Algorithm," *2001 IEICE Communication Society Conference*, B-1-34, University of Electro-Communications, Chofu, JAPAN, Sep. 2001 (in Japanese).
29. Shintaro Muramatsu, Minseok Kim and Hiroyuki Arai, "Optimal Bit Length of Fixed-Point Computation in Eigenvalue Decomposition for MUSIC Algorithm," *2002 IEICE General Conference*, B-1-18, Waseda University, Tokyo, JAPAN, Mar. 2002 (in Japanese).
30. Aiko Kiyono, Minseok Kim, Koichi Ichige and Hiroyuki Arai, "Effect of Sampling Jitter on Digital Downconversion Receiver," *2004 IEICE Society Conference*, B-17-2, Tokushima University, Shikoku, JAPAN, Sept. 2004 (in Japanese).
31. Atsushi Nakajima, Minseok Kim and Hiroyuki Arai, "Performance evaluation of MMSE adaptive array with FPGA," *2004 IEICE Society Conference*, B-5-78, Tokushima University, Shikoku, JAPAN, Sept. 2004 (in Japanese).
32. Atsushi Nakajima, Minseok Kim and Hiroyuki Arai, "Indoor propagation experiment of RLS adaptive array based on FPGA," *2005 IEICE General Conference*, Osaka University, Osaka, JAPAN, Mar. 2005 (in Japanese, submitted).